CASE STUDY ON FAMILIES OF ARM PROCESSORS

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ABSTRACT:

ARM is a family of instruction set architectures for computer processors based on RISC architecture developed by British company ARM Holdings. A RISC-based computer design approach means ARM processors require significantly fewer transistors than typical CISC x86 processors in most personal computers. This approach reduces costs, heat and power use. These are desirable traits for light, portable, battery-powered devices—including smartphones , laptops, tablet and notepad computers, and other embedded systems. A simpler design facilitates more efficient multi-core CPUs and higher core counts at lower cost, providing improved energy efficiency for servers. .[1][2] [3] In this paper would study about various ARM family members that includes ARM 7/9/11, Cortex A, and Cortex M.

Keywords: ARM 7,ARM 9,ARM 11,

I.INTRODUCTION

ARM Holdings develops the instruction set and architecture for ARM-based products, but does not manufacture products. The company periodically releases updates to its cores. Current cores from ARM Holdings support a 32-bit address space and 32-bit arithmetic; the recently introduced ARMv8-A architecture adds support for a 64-bit address space and 64-bit arithmetic. Instructions for ARM Holdings' cores have 32-bit-wide fixed-length instructions, but later versions of the architecture also support a variable-length instruction set that provides both 32-bit and 16-bit-wide instructions for improved code density. Some cores can also provide hardware execution of Java bytecodes.

ARM Holdings licenses the chip designs and the ARM instruction set architectures to third-parties, who design their own products that implement one of those architectures—including systems-on-chips (SoC) that incorporate memory, interfaces, radios, etc. Currently, the widely used Cortex cores , older "classic"cores,and specialized SecurCore cores variants are available for each of these to include or exclude optional capabilities. Companies that produce ARM products include Apple, Nvidia, Qualcomm, Rockchip, Samsung Electronics, and Texas Instruments. Apple first implemented the ARMv8-A architecture in the Apple A7 chip in the iPhone 5S.

In 2005, about 98% of all mobile phones sold used at least one ARM processor.[4] The low power consumption of ARM processors has made them very popular: 37 billion ARM processors have been produced as of 2013, up from 10 billion in 2008.[5] The ARM architecture (32-bit) is the most widely used architecture in mobile devices, and most popular 32-bit one in embedded systems.[6]

According to ARM Holdings, in 2010 alone, producers of chips based on ARM architectures reported shipments of 6.1 billion ARM-based processors , representing 95% of smartphones , 35% of digital televisions and set-top boxes and 10% of mobile computers. It is the most widely used 32-bit instruction set architecture in terms of quantity produced. [7][8]

II. ARM 7

Introduced in 1994, the ARM7™ processor family has been immensely successful, and has helped establish ARM as the architecture of choice in the digital world. Over the years, more than 10 billion ARM7 processor family-based devices have powered a wide variety of cost and power-sensitive applications.

While the ARM7 processor family continues to be used today for simple 32-bit devices, newer embedded designs are increasingly making use of latest ARM processors such as the Cortex™-M0 and Cortex-M3 processors, both of which offer significant technical enhancements over the ARM7 family.

ARM7500

It is a highly integrated single chip computer based around the ARM RISC microprocessor macrocell. ARM7500 contains all the functionality required to create a complete computing system with the minimum of external components. The wide range of features incorporated into ARM7500 make it an extremely flexible device, which can be programmed according to the required application to optimise for high performance or low power, or a combination of both.

Features

n Highly integrated RISC computer

n 30 Dhrystone 2.1 MIPS ARM7 core @ 33MHz

n 4 Kbyte combined instruction and data cache

n Flexible Memory Management Unit

n Supports 16 or 32 bit wide memory via internal ROM and DRAM controllers

n 3 channel DMA

n I/O controller

n 2 serial ports, 4 A/D channels

n 8 stereo sound channels

n 32-bit CD quality serial sound channel

n Video controller with up to 120MHz pixel clock

n 16 million colours from 256-entry palette

n 16-level grey scales for LCD displays

n Suspend and stop power saving modes

Applications

ARM7500 is ideally suited to those applications requiring a compact, low-cost, power-efficient, high performance, RISC computing system on a single chip. These include: Multimedia Interactive visual display terminals, Portable Computing Handheld test instrumentation, Games consoles Desktop computing.

ARM7DI

Is a low-power, general purpose 32-bit RISC microprocessor with integrated debug support.

It comprises the ARM7D CPU core, and ICE breaker module and a TAP controller. Its simple, elegant and fully static design is particularly suitable for cost and power sensitive applications.

Enhancements

The ARM7DI is similar to the ARM6 but with the following enhancements:

n advanced debug (integrated ICE) support for faster time to market

n fabrication on a sub-micron process for increased speed and reduced power consumption

n 3V operation, for very low power consumption, as well as 5V operation for system compatibility

n higher clock speed for faster program execution.

Applications

The ARM7DI is ideally suited to those applications requiring RISC performance from a compact, power-efficient processor. These include:

Telecomms GSM terminal controller

Datacomms Protocol conversion

Portable Computing Palmtop computer

Portable InstrumentS Handheld data acquisition unit

Automotive Engine management unit

Information Systems Smart cards

Imaging JPEG controller

ARM710T

The ARM710T is a general-purpose 32-bit microprocessor with 8KB cache, enlarged write buffer and Memory Management Unit (MMU) combined in a single chip. The CPU within the ARM710T is the ARM7TDMI. The ARM710T is software compatible with the ARM processor family.

The ARM710T architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are greatly simplified compared with microprogrammed Complex Instruction Set Computers (CISC).

The on-chip mixed data and instruction cache, together with the write buffer, substantially raise the average execution speed and reduce the average amount of memory bandwidth required by the processor. This allows the external memory to support additional processors or Direct Memory Access (DMA) channels with minimal performance loss.

The MMU supports a conventional two-level page-table structure and a number of extensions which make it ideal for embedded control, UNIX and Object Oriented systems.

The memory interface has been designed to allow the performance potential to be realised without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals permit the exploitation of paged mode access offered by industry standard DRAMs. ARM710T is a fully static part and has been designed to minimise power requirements.

This makes it ideal for portable applications where both these features are essential.

III. ARM 9

With this design generation, ARM moved from a von Neumann architecture (Princeton architecture) to a Harvard architecture with separate instruction and data buses (and caches), significantly increasing its potential speed. Most silicon chips integrating these cores will package them as modified Harvard architecture chips, combining the two address buses on the other side of separated CPU caches and tightly coupled memories.

There are two subfamilies, implementing different ARM architecture versions.

Differences from ARM7 cores

Key improvements over ARM7 cores, enabled by spending more transistors, include:[1]

- Decreased heat production and lower overheating risk.
- Clock frequency improvements. Shifting from a three-stage pipeline to a five-stage one lets the clock speed be approximately doubled, on the same silicon fabrication process.
- Cycle count improvements. Many unmodified ARM7 binaries were measured as taking about 30% fewer cycles to execute on ARM9 cores. Key improvements include:
- Faster loads and stores; many instructions now cost just one cycle. This is helped by both the modified Harvard architecture (reducing bus and cache contention) and the new pipeline stages.
- Exposing pipeline interlocks, enabling compiler optimizations to reduce blockage between stages.

Additionally, some ARM9 cores incorporate "Enhanced DSP" instructions, such as a multiply-accumulate, to support more efficient implementations of digital signal processing algorithms.

Switching to a Harvard architecture entailed a non-unified cache, so that instruction fetches do not evict data (and vice versa). ARM9 cores have separate data and address bus signals, which chip designers use in various ways. In most cases they connect at least part of the address space in von Neumann style, used for both instructions and data, usually to an AHB interconnect connecting to a DRAM interface and an External Bus Interface usable with NOR flash memory. Such hybrids are no longer pure Harvard architecture processors.

VFP9-S

The VFP9-S coprocessor is an implementation of the Vector Floating-point Architecture (VFPv2). It provides low-cost floating-point computation that is fully compliant with the ANSI/IEEE Std 754-1985, IEEE Standard for Binary Floating-Point Arithmetic, referred to in this document as the IEEE 754 standard. The VFP9-S coprocessor supports all addressing modes described in the ARM Architecture Reference Manual.

The VFP9-S coprocessor is optimized for:

• high data transfer bandwidth through 32-bit split load and store buses

• fast hardware execution of a high percentage of operations on normalized data resulting in higher overall performance while providing full IEEE 754 standard support when required

• divide and square root operations in parallel with other arithmetic operations to reduce the impact of long-latency operations

• near IEEE 754 standard compatibility in RunFast mode without support code assistance, providing determinable run-time calculations for all input data

• low power consumption, small die size, and reduced kernel code.

The VFP9-S coprocessor is an ARM enhanced numeric coprocessor that provides IEEE 754 standard-compatible operations. It is designed to be incorporated with the ARM9E

family of processors, ARM9E-S, ARM9EJ-S, ARM926EJ-S, ARM946E-S, and ARM966E-S. It provides full support of single-precision and double-precision add, subtract, multiply, divide, and multiply with accumulate operations. Conversions between floating-point data formats and ARM integer word format are provided, with special operations to perform the conversion in round-toward-zero mode for high-level language support.

The VFP9-S coprocessor provides a performance-power-area solution for embedded applications and high performance for general-purpose applications, such as Java.

ARM922T

The ARM922T macrocell is a high-performance 32-bit RISC integer processor combining an ARM9TDMI™ processor core with:

- 8KB instruction cache and 8KB data cache
- instruction and data *Memory Management Unit* (MMU)
- write buffer with 16 data words and 4 addresses
- *Advanced Microprocessor Bus Architecture* (AMBA™) AHB interface
- *Embedded Trace Macrocell* (ETM) interface
- EXTEST-compatible boundary scan chain.

Benefits

- Designed specifically for System-on-Chip integration
- Supports the Thumb® instruction set offering the same excellent code density as the ARM7TDMI cores
- High performance lets system designers integrate more functionality into price and power-sensitive applications
- Cached processor with an easy-to-use lower frequency on-chip system bus interface.

MOVE coprocessor

The MOVE coprocessor is a video encoding acceleration coprocessor designed to accelerate *Motion Estimation* (ME) algorithms within block-based video encoding schemes such as MPEG4 and H.263. It provides support for the execution of *Sum of Absolute Differences* (SAD) calculations, which account for most of the processing activity within an ME algorithm. The ME algorithms require many comparisons of 8x8 pixel blocks to be made between a current frame and a reference frame.

This coprocessor is one element in the MOVE product group. It is assigned the letter U. All coprocessor instruction mnemonics are prefixed with the letter U.

The MOVE is closely coupled to the ARM9x6 family of processors. Each instruction that is destined for the MOVE is processed immediately as if the ARM core is executing the instruction.

The MOVE is not a *fire and forget* coprocessor. MOVE instructions are executed immediately and the result is available for the following instruction, subject to certain conditions. See *Data hazards*. This means that the ARM processor does not have to poll the status of the coprocessor, and the coprocessor does not have to interrupt the ARM processor.

III. ARM 11

ARM documentation set for the ARM11 family of processors, including ARM1136JF-S and ARM1126J-S, ARM1156T2-S, ARM1156T2F-S,ARM1176JZF,ARM1176JZ-S, ARM1176JZF-S, and ARM11 MPCore processors.

The ARM11 family comprises four series of processors that implement the ARM architecture v6 with extensions including a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

- **The ARM1136J-S and ARM1136JF-S** processors feature ARM Jazelle technology. They implement a Virtual Memory System Architecture and have AMBA 2 AHB interfaces. They support the ARM instruction set and the original Thumb instruction set. The ARM1136JF-S processor has a floating point coprocessor.
- **The ARM1156T2-S and ARM1156T2F-S** processors feature optional Memory Protection Units (MPUs) for instruction and data memory, optional parity protection for caches and tightly coupled memories, and have AMBA 3 AXI interfaces. They support the ARM and Thumb instruction sets, with the Thumb-2 extensions. The ARM1156T2F-S processor has a floating point coprocessor.
- **The ARM1176JZ-S and ARM1176JZF-S** processors feature ARM TrustZone technology and ARM Jazelle technology, and support ARM Intelligent Energy Manager (IEM) technology. They implement a Virtual Memory System architecture, and have AMBA 3 AXI interfaces. They support the ARM instruction set and the original Thumb instruction set. The ARM1176JZF-S processor has a floating point coprocessor.
- **The ARM11 MPCore multiprocessor** is configured to include 1-4 processors that can be viewed as a single processor. It features ARM Jazelle technology, and supports ARM IEM technology. It implements a Virtual Memory System Architecture with configurable level 1 caches, a vector floating point coprocessor, and programmable interrupt control and distribution, and has AMBA 3 AXI interfaces. It supports the ARM instruction set and the original Thumb instruction set.

IV.CORTEX A

The Cortex-A5, Cortex-A7, Cortex-A9, Cortex-A12, Cortex-A15 and Cortex-A17 processors are all used in a wide variety of performance applications. However while all support the same excellent base ARMv7-A ISA capabilities and full software compatibility, these processors offer significantly different power and performance characteristics to ensure the right-fit for tomorrow's advanced embedded solutions and wide variety of mobile and consumer applications.

Cortex-A Comparisons

All Cortex-A series processors share a common architecture and feature set. This makes them the best solution for open platform design where compatibility and portability of software between designs is of upmost importance:

- ARMv7-A architecture
- Support for full Operating Systems
- Linux full distributions- Android, Chrome, Ubuntu and Debian
- Linux 3rd party - MontaVista, QNX, Wind River
- Symbian
- Windows CE
- Other OS support requiring Memory Management Unit

- Instruction Set Support - ARM, Thumb-2, Thumb, Jazelle®, DSP
- TrustZone® Security Extensions
- Advanced single-precision and double-precision Floating Point support
- NEON™ media processing engine
- Virtualization
- 1TB addressing (LPAE)

Together, the range of Cortex-A processors provide design flexibility by providing the required peak performance points and scalability and delivering the desired power efficiency and silicon cost while maintaining full software compatibility.

Core	Cortex-A5	Cortex-A5 MPCore	Cortex-A7	Cortex-A9	Cortex-A9 MPCore	Cortex-A12	Cortex-A15	Cortex-A17
Architecture	ARM v7	ARMv7+ MP	ARMv7+ MP +LPAE	ARM v7	ARMv7+ MP	ARMv7+ MP +LPAE	ARMv7+ MP +LPAE	ARMv7+ MP +LPAE
Interrupt Controller	GIC-390	Integrated-GIC	GIC-400	GIC-390	Integrated-GIC	GIC-400	Integrated-GIC	GIC-400
L2 Cache Controller	L2C-310	L2C-310	Integrated	L2C-310	L2C-310	Integrated	Integrated	Integrated

V.CORTEX M

The ARM Cortex®-M processor family is an upwards compatible range of energy-efficient , It delivers more features at a lower cost, increasing connectivity, better code reuse and improved energy efficiency.

The Cortex-M family is optimized for cost and power sensitive MCU and mixed-signal devices for end applications such as smart metering, human interface devices, automotive and industrial control systems, white goods, consumer products and medical instrumentation.

More information on ARM embedded products and resources is available in the Embedded Group on ARM Connected Community.

Industry standard

ARM Cortex-M processors is a global microcontroller standard, having been licensed to over 40 ARM partners including leading vendors such as Freescale, NXP Semiconductors, STMicroelectronics, Texas Instruments, and Toshiba. Using a standard processor allows ARM partners to create devices with a consistent architecture while enabling them to focus on creating superior device implementations.

Energy efficiency

Lower energy costs, longer battery life

- Run at lower MHz or with shorter activity periods
- Architected support for sleep modes
- Work smarter, sleep longer than 8/16-bit

Smaller code

Lower silicon costs

- High density instruction set
- Achieve more per byte than 8/16-bit devices
- Smaller RAM, ROM or Flash requirement

Ease of use

Faster software development and reuse

- Global standard across multiple vendors
- Code compatibility
- Unified tools and OS support

Comparing Cortex-M processors

The Cortex-M family is an ideal solution for ranges of compatible, easy to use embedded devices such as microcontrollers (MCU) where different cost, power and performance are considerations. Each processor delivers an optimal trade-off for a broad embedded application range.

ARM Cortex-M0	ARM Cortex-M0+	ARM Cortex-M3	ARM Cortex-M4
"8/16-bit" applications	"8/16-bit" applications	"16/32-bit" applications	"32-bit/DSC" applications
Low cost and simplicity	Low cost, best energy-efficiency	Performance, general purpose	Efficient digital signal control

Cortex-M family processors are all binary upwards compatible, enabling software reuse and a seamless progression from one Cortex-M processor to another.

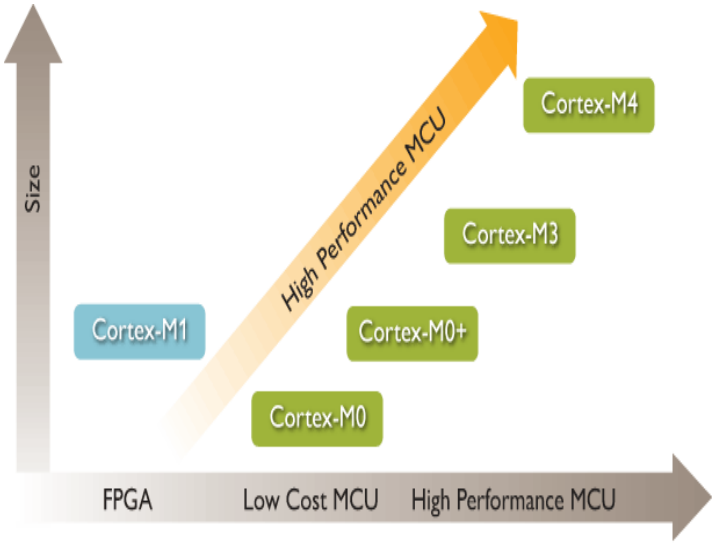

FIG 2 :Comparing Cortex -M

V.COMPARISON AMONG FAMILIES OF ARM PROCESSORS

Technology	ARM7 Family ARMv4T Architecture	ARM9 Family ARMv5TE Architecture	ARM11 Family ARMv6 Architecture
ARM ISA	Yes	Yes	Yes
Thumb ISA	Yes	Yes	Yes
Thumb-2 ISA	No	No	Yes (ARM1156T2-S Only)
DSP Extensions	No	Yes	Yes
SIMD Extensions	No	No	Yes
Jazelle Bytecode Support	No	Yes (ARM926EJ-S Only)	Yes (Except ARM1156T2-S)
Floating Point Support	No	Yes (VFP9)	Yes (VFP11)
TrustZone Security Extensions	No	No	Yes (ARM1176JZ(F)-S Only)
Cache Support	No	Yes	Yes
TCM Support	No	Yes	Yes

5.CONCLUSION

In this paper we studied about the families of ARM processors, their benefits and their applications.We also compared the ARM 7,ARM 9 and ARM 11 available in order to get a deeper insight into the hardware and software specification.

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