Analysis and Design of Impulse-Commutated Zero-Current-Switching Single-Inductor Current-Fed Three-Phase Push–Pull Converter

LAKKAM ASHOK[1] & YENISETTI NEELIMA[2]
ASSISTANT PROFESSORS
DEPT OF EEE
CHRISTU JYOTHI INSTITUTE OF TECHNOLOGY AND SCIENCE
YASHWANTHAPUR, JANGOAN T.S

***Abstract*—Impulse commutation obtains zero current commutation of devices in a circuit with a short resonance impulse using a simple resonant tank. This concept has been studied, extended, and implemented for a three-phase push–pull current-fed single-inductor topology to achieve soft commutation and device voltage clamping solving the traditional issue of device turn-off voltage overshoot. The push–pull topology is attractive owing to single in-ductor, all common source devices connected to common supply ground, and reduced gate driving requirements. Detailed opera-tion, analysis, and design of this topology have been reported with impulse commutation. With a small resonant tank and partial reso-nance, impulse commutation procures merits of voltage clamping, low circulating current, and load adaptive zero-current switch-ing of the devices. Variable-frequency modulation regulates load voltage and maintains the impulse commutation with source volt-age variation. Experimental results on a 1-kW proof-of-concept hardware prototype are demonstrated to observe the operation, performance, and verify the proposed concept and claims.**

***Index Terms*—Current-fed converter, dc/dc power conversion, impulse commutation, three-phase, zero-current switching (ZCS).**

I. INTRODUCTION

CURRENT-FED power electronic circuits are boost-derived converters and have been justified for voltage gain and low-voltage high-current applications [1]. Like traditional voltage-fed topologies, identical current-fed topologies exist, and the major scope of research is analysis and design of these topologies with new modulation and soft-switching techniques. Novel modulation and auxiliary circuits are often investigated to solve the traditional problems associated with the topology and enhance the circuit performance for given application and specifications. Current-fed circuits offers high voltage gain, inherent short-circuit protection, limit peak and circulating current through the devices and components, reduced transformer size

in the case of isolated converters, and reduced source current ripple [2], [3]. Current limiting and short-circuit protection are important for high-current applications. In addition, an induc-tor is reliable and has higher life than an electrolytic capacitor employed in voltage-fed converters. and the voltage spikes across devices at their turn-off are the two major limitations that override the extraordinary merits.

The merits of current-fed circuits open scope for their several emerging applications. However, charging the inductor at star Tradi-tionally, dissipative snubbers [4], [5] have been used to reduce the device turn-off voltage spike by compromising on the con-version efficiency. Active-clamp solution offers high efficiency and soft switching [6] but compromises on voltage gain and modularity of the circuits introducing circuit complexity owing to floating active devices.

Naturally commutated topologies with secondary modulation concept have been reported in [7] to limit the device voltage at reflected output voltage naturally with zero-current commutation. Boost capacity and originality of the circuits are preserved with high efficiency. However, these topologies require active devices on the load side and, therefore, are suitable for bidirectional applications because of active device count and driving requirements. Unidirectional converters are simple in circuit and control implementation if diodes are placed on the load side for rectification. Resonant tanks have been adopted to develop resonant converters by voltage-fed buck-derived circuits. However, in resonant converters, owing to circulating current, peak (above 2×) and rms current through the devices and components are high. This makes the ratings of the components high and their selection difficult for low-voltage high-current applications. Also, implementing the concept to current fed is not as straightforward owing to the different fundamental nature of the circuits.

In current-fed circuits, hard commutation is a major issue, as it results in device voltage overshoot. Instead of full resonance, partial resonance at turn-off may obtain the benefits of soft commutation and limit the device voltage along with limited peak and circulating current. It introduces the concept of impulse commutation, which is a short resonance impulse during turn-off to commutate the device softly with zero current. The idea has been studied, extended, and implemented for current-fed circuits, introducing a family of impulse-commutated current-fed converters.

Based on specifications and applications, single-phase and three-phase topologies, mainly full-bridge [8], half bridge [9],

TABLE I
COMPARISON OF THE PROPOSED IMPULSE-COMMUTATED TOPOLOGY WITH OTHER THREE-PHASE PUSH–PULL TOPOLOGIES

	Impulse Commutation	Active clamping	Passive snubbing
Modulation	Variable frequency	Duty cycle	Duty cycle
Modes of operation	Only CCM	Both CCM and DCM	Both CCM and DCM
Switching method	Soft-switching (ZCS)	Soft-switching (ZVS)	Hard switching
Diode reverse recovery	Negligible	Negligible	Considerable
Circuit complexity	Simple	Complex	Simple
Additional devices	Parallel capacitors	three high-side device	Passive snubbers
Clamping method	Naturally Clamped	Active clamping	Passive clamping (RCD)
Duty cycle	$0.33 < D < 0.66$	$D < 0.33$ $0.33 < D < 0.66$ $D > 0.66$	$0.33 < D < 0.66$ $D > 0.66$
No. of. conducting devices	Upto 2 ($0.33 < D < 0.66$)	Upto 4 ($D < 0.33$) Upto 4 ($0.33 < D < 0.66$) Upto 4 ($D > 0.66$)	Upto 2 ($0.33 < D < 0.66$) Upto 4 ($D > 0.66$)
Device voltages	Short resonance impulse to V_o/n	$V_{in,min}/(1-D_{max})$	$V_{in,min}/(1-D_{max})$

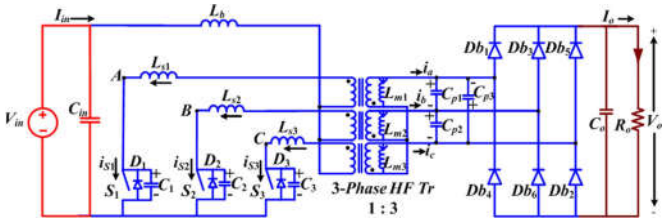


Fig. 1. Proposed impulse-commutated three-phase current-fed push–pull dc/dc converter.

[10], and push–pull [7], have been reported in the literature. Six-pack topology [11] is preferred over push–pull for high-power application because of modularity and reduced transformer kVA rating. Current sharing topology [12], [13] is preferred for higher current applications owing to current sharing, reduced device current stress, and reduced transformer kVA rating. The push–pull topology is suitable for medium-power applications and is attractive owing to these reasons: 1) reduced gate driving requirements owing to the low-side primary devices; and 2) high voltage gain with a single inductor.

The three-phase equivalent of the push–pull topology was first proposed in [14]. Input and output filtering requirements are significantly lower in the three-phase equivalent, as the chopping frequency is thrice the switching frequency [15]. The three-phase equivalent circuit offered high power density [16], [17] with reduced device current and voltage stresses. However, the historic issue of turn-off device voltage spike in current-fed converters prevailed [18].

In the literature for three-phase configurations, the turn-off device voltage spike across the semiconductor devices has been addressed using snubbers [19], active-clamp circuits [6], [8], [13], and secondary modulation [20]. As pointed out earlier, with limitations imposed on the frequency of operation due to hard switching, passive snubbers depreciate the converter's efficiency and increase the volume at the same time. Active-clamp circuits facilitate voltage clamping of devices along with zero voltage switching (ZVS) [6], [8] while reducing the con-verter's boost capacity and increasing the circuit complexity and required high-side devices. Secondary modulation offers natural clamping and zero-current commutation of the devices; however, such converters tend to be expensive for unidirectional applications due to increased high-side switches and driver circuits. Impulse commutation helps resolve this issue for unidirectional applications in simple and cost-effective way without increasing the circuit complexity and compromising on the performance. It should be noted that so far in the literature, the current-sharing three-inductor three-phase converter topology [21] and the single-phase current-fed push–pull topology with impulse commutation [22] have been analyzed and reported. However, the three-phase single-inductor push–pull current-fed topology with impulse commutation has not been studied and explored.

This paper studies, analyzes, and designs this topology with impulse commutation. The proposed impulse-commutated three-phase single-inductor current-fed push–pull topology has also been compared with other three-phase push–pull converters with active clamp and passive snubbers in Table I to benchmark. From Table I, it can be inferred that the proposed commutation strategy employs additional high-frequency (HF) ceramic ca-pacitors, and the energy stored in them facilitates zero-current switching (ZCS) during resonance with natural voltage clamp-ing of the semiconductor devices [21]–[24]. The resonance ex-ploits the transformer parasitics, the leakage inductance, and the parasitic capacitance to positively impact the converter per-formance, and an analysis is done to achieve the desired goals. The technique is thus simple and cost effective and enhances the converter performance and efficiency.

It should be noted that in this paper, the concept of impulse commutation is extended to analyze and design a single-inductor three-phase push–pull current-fed converter shown in Fig. 1. The circuit configuration and operation is different from the current-sharing topology proposed in [21]. With a few similarities in-cluding the expression for the voltage gain, etc., the notable differences between the proposed topology and the current-sharing topology proposed in [21] are the following.

1) The switch and the series inductor currents in the proposed topology are identical, while they have different values and waveforms in other topology.
2) The dc voltage gain is comparable to the current-sharing topology despite using a single boost/input inductor.

3) For the same specifications, the reduction in volume of magnetics is evident in the proposed topology.

The objectives of this paper have been realized in several sections. Steady-state operation and analysis of the three-phase single-inductor current-fed push–pull topology with impulse commutation are explored and reported in Section II. A systematic design procedure to determine the component value and rating to develop the impulse-commutation circuit for given specifications is illustrated in Section III. A proof-of-concept laboratory hardware prototype rated at 1 kW is developed in lab and tested to demonstrate the performance and the claims. Experimental results are presented in Section IV.

II. OPERATION AND STEADY-STATE ANALYSIS

This section studies the steady-state operation and analysis of the proposed impulse-commutated converter. For simplifying the converter analysis, the following assumptions are made.

1) Input boost inductor L_b carries a stiff dc current.
2) All semiconductor devices are ideal and lossless.
3) The leakage inductance of the HF transformers and the additional capacitance between the phases included for impulse commutation are equal, i.e., $L_{s1} = L_{s2} = L_{s3} = L_s$ and $C_{p\,1} = C_{p\,2} = C_{p\,3} = C_p$, and the magnetizing inductances referred to the secondary of the HF transformers ($L_{m\,1} = L_{m\,2} = L_{m\,3} = L_m$) are considerable and they carry a constant current $I_{in}/3n$.

Variable-frequency modulation exercises control over the power transfer and voltage regulation under all operating conditions. The gating signal to the devices are phase shifted by 120° with an overlap decided by the constant duty cycle D. D is necessarily greater than 33%, with the maximum possible value being 66%. The analysis has been carried out for one-third of the HF cycle. For the other subsequent cycles, the intervals re-peat in the same sequence with the other symmetrical devices conducting. The equivalent circuits depicting the different inter-vals of operation and the steady-state operating waveforms are in Figs. 2 and 3, respectively.

A. Interval 1 (Fig. 2(a): $t_0 < t < t_1$)—Power Transfer

In this mode, the primary switch S_1 and the rectifier diodes D_{b1}, D_{b2}, and D_{b6} transfer power to the load. Switch S_1 con-ducts the input current I_{in} with the voltage across the parallel capacitor $C_{p\,1}$ clamped at V_o. The reflected input current gets divided equally between the three magnetizing inductances, i.e., $I_{in}/3n$ flows through them. Constant current $2I_{in}/3n$, $-I_{in}/3n$, and $-I_{in}/3n$ flows through the phases A, B, and C in the sec-ondary. Final values are: $i_{L\,s1}(t_1) = i_{S\,1}(t_1) = I_{in}$; $v_{C\,p\,1}(t_1) = V_o$; $v_{C\,p\,2}(t_1) = 0$; $v_{C\,p\,3}(t_1) = -V_o$; $i_a(t_1) = 2I_{in}/3n$; $i_b(t_1) = i_c(t_1) = -I_{in}/3n$.

B. Interval 2 (Fig. 2(b): $t_1 < t < t_2$)—Device Capacitance Discharges

At $t = t_1$, switch S_2 is turned ON. Thereafter, the device capacitance C_2 discharges through the switch in a very short duration of time.

C. Interval 3 (Fig. 2(c): $t_2 < t < t_3$)—Power Transfer

With the primary switch S_2 gated-on in the previous interval, S_2 commences to take over the input current I_{in} from S_1. Thereby, the current through the series inductors L_{s1} and L_{s2}, and hence, the respective switches starts decreasing and increas-ing, respectively, with a slope of $V_o/2nL_s$. These currents can be given as

$$i_{L\,s1}(t) = i_{S\,1}(t) = I_{in} - \frac{V_o}{2nL_s}(t - t_2) \quad (1)$$

$$i_{L\,s2}(t) = i_{S\,2}(t) = \frac{V_o}{2nL_s}(t - t_2). \quad (2)$$

With the rectifier diodes D_{b1}, D_{b2}, and D_{b6} transferring power to the load, the secondary phase currents can be given as

$$i_a(t) = \frac{i_{L\,s1}(t)}{n} - \frac{I_{in}}{3n} \quad (3)$$

$$i_b(t) = \frac{i_{L\,s2}(t)}{n} - \frac{I_{in}}{3n}. \quad (4)$$

Constant current $-I_{in}/3n$ flows through phase C on the secondary side. At the end of the interval, one of the rectifier diodes D_{b6} commutes as the secondary current in phase B (i_b) reaches zero. Final values are: $i_{L\,s1}(t_3) = i_{S\,1}(t_3) = 2I_{in}/3$; $i_{L\,s2}(t_3) = i_{S\,2}(t_3) = I_{in}/3$; $v_{C\,p\,1}(t_3) = V_o$; $v_{C\,p\,3}(t_3) = -V_o$; $v_{C\,p\,2}(t_3) = 0$; $i_a(t_3) = I_{in}/3n$; $i_b(t_3) = 0$, and $i_c(t_3) = -I_{in}/3n$. The duration of this interval is given as

$$T_{3\,2} = (t_3 - t_2) = \frac{2nI_{in}L_s}{3V_o}. \quad (5)$$

D. Interval 4 (Fig. 2(d): $t_3 < t < t_4$)—Resonance Impulse

The primary switches S_1 and S_2 continue to conduct. The resonance between the series inductors L_{s1} and L_{s2} and the parallel capacitor $C_{p\,1}$ commences during this interval. The switch currents now increase and decrease in a resonant fashion. The resonant frequency and the characteristic impedance can be given as

$$f_r = \frac{1}{2\pi\sqrt{L_{eq}C_p}} \quad (6)$$

$$Z_r = \sqrt{\frac{L_{eq}}{C_p}} \quad (7)$$

where L_{eq} can be given as $L_{s1} + L_{s2}$ and C_p is the parallel capacitance reflected to the primary. The switch currents can be given as

$$i_{L\,s1}(t) = i_{S\,1}(t) = \frac{2I_{in}}{3} - \frac{V_o}{nZ_r}\sin(2\pi f_r(t - t_3)) \quad (8)$$

$$i_{L\,s2}(t) = i_{S\,2}(t) = \frac{I_{in}}{3} + \frac{V_o}{nZ_r}\sin(2\pi f_r(t - t_3)). \quad (9)$$

The current i_b increases in the positive direction, and this cur-rent discharges and charges $C_{p\,1}$ and $C_{p\,2}$. The secondary phase currents i_a and i_b can be given by (3) and (4), respectively. At the end of the interval, the input current gets shared equally between the two switches. Final values are: $i_{L\,s1}(t_4) = i_{L\,s2}$

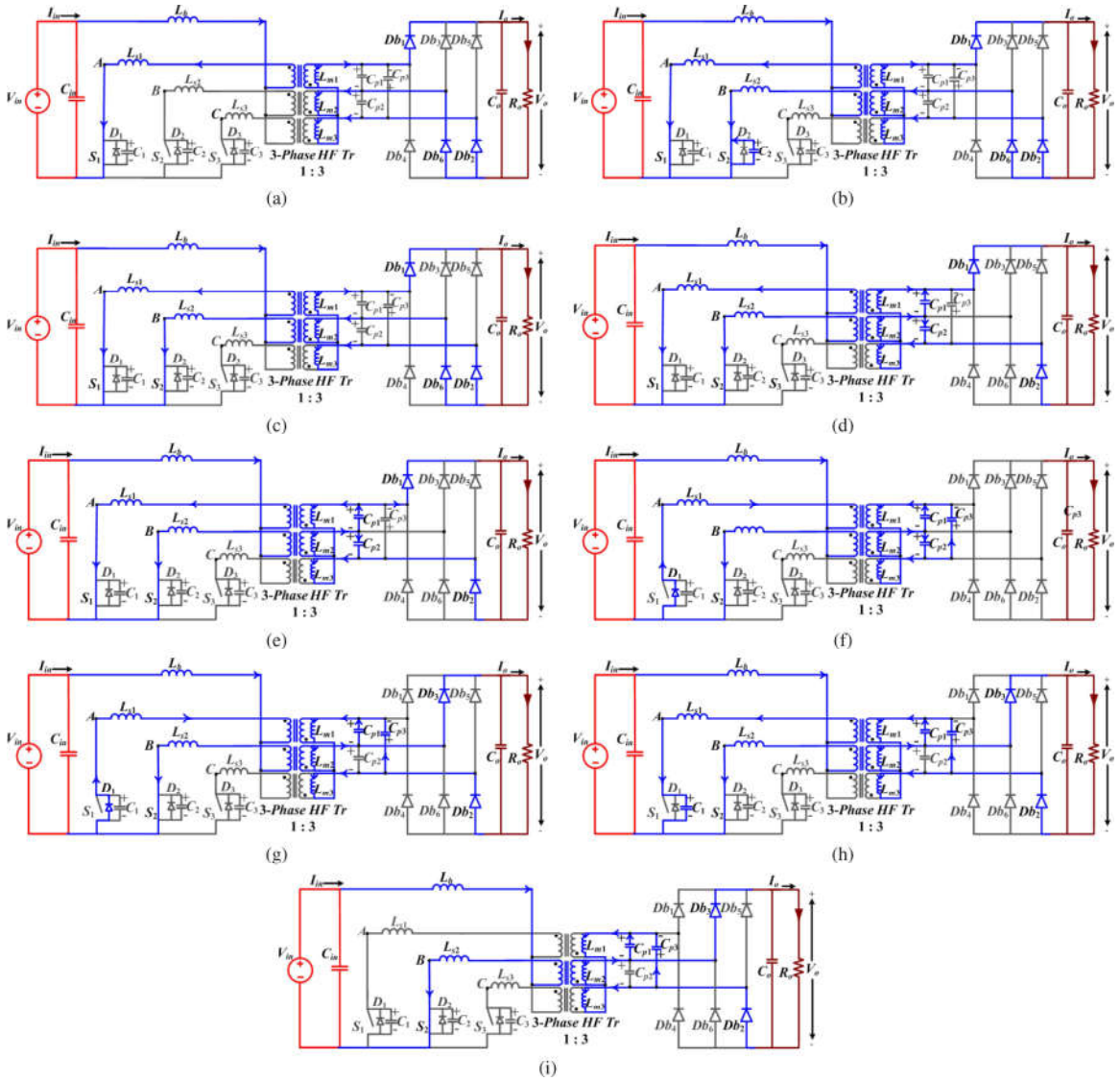


Fig. 2. Equivalent circuits representing the different intervals of operation of the proposed converter.

$(t_4) = i_{S1}(t_4) = i_{S2}(t_4) = I_{in}/2$; $v_{Cp3}(t_4) = -V_o$; $i_a(t_4) = I_{in}/6n$; $i_b(t_4) = I_{in}/6n$; and $i_c(t_4) = -I_{in}/3n$. The duration of this interval can be given as

$$T_{43} = (t_4 - t_3) = \frac{1}{2\pi f_r}\sin^{-1}\frac{nI_{in}Z_r}{6V_o} \qquad (10)$$

E. Interval 5 (Fig. 2(d): $t_4 < t < t_5$)—Resonance Impulse

The primary switches S_1 and S_2 continue to conduct during this interval. The current through S_2 increases beyond $I_{in}/2$, while current through S_1 decreases below $I_{in}/2$. The currents can be given as

$$i_{Ls1}(t) = i_{S1}(t) = \frac{I_{in}}{2} - \frac{V_o}{nZ_r}\sin(2\pi f_r(t - t_4)) \qquad (11)$$

$$i_{Ls2}(t) = i_{S2}(t) = \frac{I_{in}}{2} + \frac{V_o}{nZ_r}\sin(2\pi f_r(t - t_4)). \qquad (12)$$

At the end of the interval, the secondary current i_a reaches zero. The final values are: $i_{Ls1}(t_5) = i_{S1}(t_5) = I_{in}/3$; $i_{Ls2} = i_{S2} = 2I_{in}/3$; $v_{Cp3}(t_5) = -V_o$; $i_a(t_5) = 0$; $i_b(t_5) = I_{in}/3n$; and $i_c(t_5) = -I_{in}/3n$. The duration of this interval can be given as

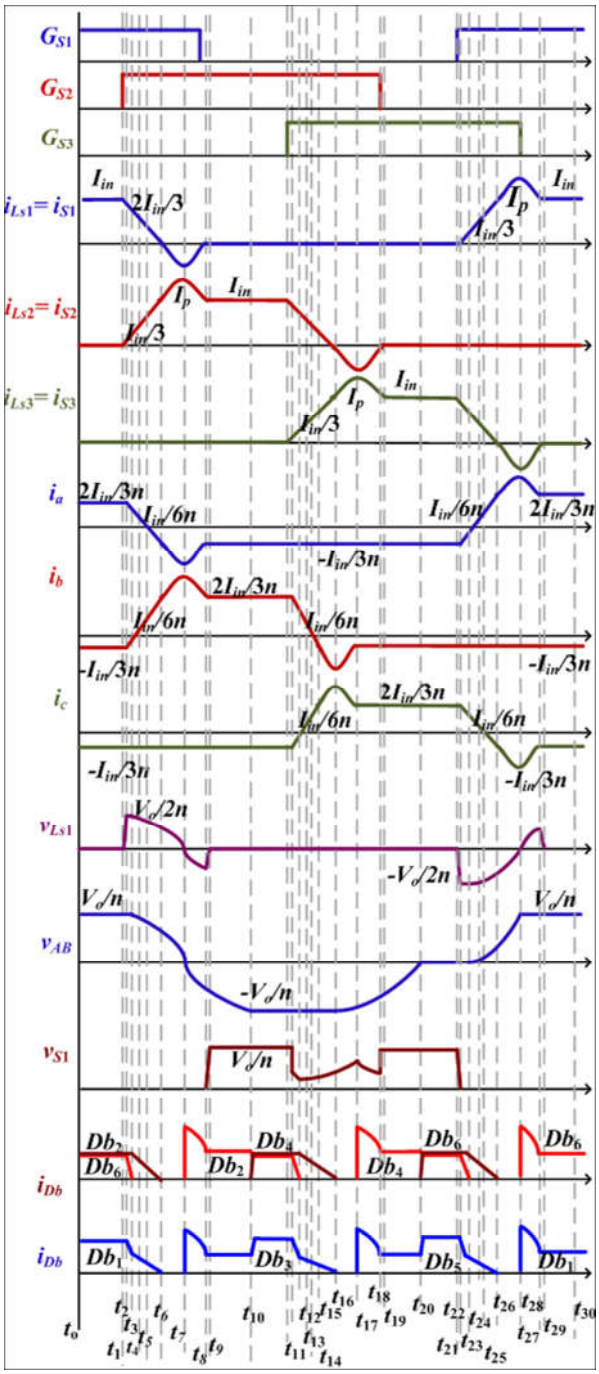
$$T_{54} = (t_5 - t_4) = \frac{1}{2\pi f_r}\sin^{-1}\frac{nI_{in}Z_r}{6V_o} \qquad (13)$$

F. Interval 6 (Fig. 2(e): $t_5 < t < t_6$)—Resonance Impulse

During this interval, the switch currents i_{S1} and i_{S2} continue to decrease and increase in a resonant fashion. They can be given as

$$i_{Ls1}(t) = i_{S1}(t) = \frac{I_{in}}{3} - \frac{V_o}{nZ_r}\sin(2\pi f_r(t - t_4)) \qquad (14)$$

$$i_{Ls2}(t) = i_{S2}(t) = \frac{2I_{in}}{3} + \frac{V_o}{nZ_r}\sin(2\pi f_r(t - t_4)). \qquad (15)$$



Steady-state operating waveforms of the proposed converter.

At the end of the interval, the diodes D_{b1} and D_{b2} get reverse biased as i_{S1} reaches zero. The final values are: $i_{Ls1}(t_6) = i_{S1}(t_6) = 0$; $i_{S2}(t_6) = i_{Ls2}(t_6) = I_{in}$; $v_{Cp3}(t_6) = -V_o$; $i_a(t_6) = i_c(t_6) = -I_{in}/3n$; and $i_b(t_6) = 2I_{in}/3n$. The duration of this interval can be given as

$$T_{65} = (t_6 - t_5) = \frac{1}{2\pi f_r}\sin\frac{nI_{in}Z_r}{3V_o}. \quad (16)$$

G. Interval 7 (Fig. 2(f): $t_6 < t < t_7$)—Body-Diode Conduction

The conduction of the antiparallel body diode of switch S_1 can be witnessed in this interval as i_{S1} increases in the negative direction. The switch S_1 can be turned OFF with ZCS during body-diode conduction. The current through S_2 increases above I_{in} and approaches the peak I_p, and thereby, the condition for ZCS can be formulated as

$$I_p = |i_{Ls}(t)|_{max} = \frac{2I_{in}}{3} + nZ_r \geq I_{in}. \quad (17)$$

The parallel capacitor C_{p3} also starts charging during this inter-val. At the end of the interval, i_{S2} reaches its peak value I_p and the rectifier diodes D_{b3} and D_{b2} go forward biased clamping v_{Cp2} at V_o. The final values are: $i_{Ls2}(t_7) = i_{S2}(t_7) = I_p$; $i_a(t_7) = (2I_{in}/3 - I_p/n)$; $i_b(t_7) = (I_p/n - I_{in}/3n)$; and $i_c(t_7) = -I_{in}/3n$.

H. Interval 8 (Fig. 2(g): $t_7 < t < t_8$)—ZCS Turn-Off

The body diode of the switch S_1 continues to conduct during this interval. Switch S_1 has been turned OFF with ZCS. At the end of the interval, i_{Ls1} reaches zero ceasing the body-diode conduction and i_{S2} reaches I_{in}. The final values are: $i_{Ls1}(t_8) = i_{S1}(t_8) = 0$; $i_{Ls2}(t_8) = i_{S2}(t_8) = I_{in}$; $v_{Cp2}(t_8) = V_o$; $i_a(t_8) = i_c(t_8) = -I_{in}/3n$; and $i_b(t_8) = 2I_{in}/3n$. The duration of this interval can be given as

$$T_{86} = (t_8 - t_6) = \frac{\pi - 2\pi f_r(T_{65} + T_{53})}{2\pi f_r}. \quad (18)$$

I. Interval 9 (Fig. 2(h): $t_8 < t < t_9$)—Charging of Device Capacitance

During this interval, the device capacitance C_1 of the switch S_1 charges to a maximum voltage of V_o/n from 0.

J. Interval 10 (Fig. 2(i): $t_9 < t < t_{10}$)—Charging and Discharging of Parallel Capacitors

During this interval, constant current I_{in} flows through the switch S_2 and the series inductor L_{s2}. Constant current $I_{in}/3n$, $2I_{in}/3n$, and $I_{in}/3n$ flows through the secondary in phase A, B, and C, respectively. At the end of the interval, the rectifier diode D_{b4} gets forward biased. The final values are: $i_{Ls2}(t_{10}) = i_{S2}(t_{10}) = I_{in}$; $v_{Cp3}(t_{10}) = 0$; $v_{Cp2}(t_{10}) = V_o$; $v_{Cp1}(t_{10}) = -V_o$; $i_a(t_{10}) = i_c(t_{10}) = -I_{in}/3n$; and $i_b(t_{10}) = 2I_{in}/3n$. The duration of this interval can be given as

$$T_{109} = (t_{10} - t_9) = \frac{C_p R_L}{n^2}. \quad (19)$$

At any given instant, one of the HF transformers operates like a flyback transformer storing energy in the magnetizing inductance as evident from the equivalent circuits shown in Fig. 2.

In the case of three single three-phase transformers connected in star–star configuration, the dc-shifted current in L_m leads to unidirectional core excitation. Core excitation becomes unidirectional, as the three windings are wound on separate cores inhibiting flux cancellations.

TABLE II
SPECIFICATIONS OF THE PROPOSED CONVERTER

Parameters	Values
Input voltage V_{in}	42 to 48 V
Output dc voltage V_o	380 V
Output power P_o	1 kW
Switching frequency band f_s	75–87 kHz

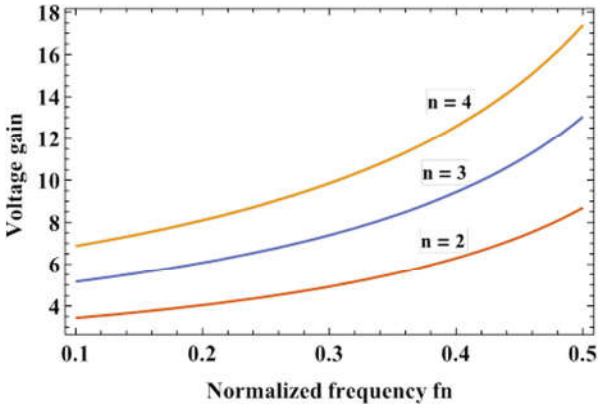


Fig. 4. Variation of the converter gain with normalized frequency f_n for different turns ratio n.

III. CONVERTER DESIGN

This section illustrates the design of the proposed impulse-commutated converter with a design example. The converter specifications are given in Table II.

A. DC Voltage Gain

The approximate and simplified expression for the dc voltage gain of the converter can be given as

$$M = \frac{V_o}{V_{in}} = \frac{n\eta}{\frac{2}{3} - 0.88 f_n} \quad (20)$$

where f_n is the normalized frequency defined as the ratio of the switching to the resonant frequency, i.e., f_s / f_r , and η is the efficiency. The variation in the converter s gain with turn ratio has been shown in Fig. 4. The band of operating frequency widens with increase in the turns ratio of the transformer for the same value of gain, load, and source voltage conditions.

B. Voltage and Current Ratings

The voltage stress across the semiconductor devices and the parallel capacitors is as follows:

$$v_{S1} \sim V_{S3} = \frac{V_o}{n} \quad (21)$$

$$V_{Db1} \sim V_{Db6} = V_o \quad (22)$$

$$V_{Cp1} \sim V_{Cp3} = V_o \quad (23)$$

TABLE III
VARIATION IN CIRCUIT PARAMETERS WITH TURNS RATIO

Turns ratio n	Switch voltage (V)	frequency f_s (kHz)
2	190	75–80
3	126.7	75–87
4	95	75–120.5

The approximate expressions for the rms current through the switches and the series inductors are given as

$$I_{Sw,rms} = I_{Ls,rms} = I_{in}\sqrt{\frac{2f_n}{9} + D - \frac{2f_n}{3}} \quad (24)$$

The rms current through the switches and, hence, the series inductors for V_{in} = 48 V and V_{in} = 42 V are computed to be 12.7 and 14.2 A, respectively. The average current through the rectifier diodes is I_o /3 and is computed as 0.88 A.

C. Selection of Turns Ratio of the HF Transformer

The transformer turns ratio determines the range of frequency variations, as evident from (20), and also determines the volt-age appearing across the primary switches, as tabulated in Ta-ble III. With a lower value of turns ratio, the device voltages are considerably high, mandating the use of high-voltage devices with higher $R_{ds,on}$. This escalates the conduction losses on the high-current side. On the other hand, higher value of turns ra-tio increases the losses in the HF transformer. From Fig. 4, the frequency variations required to operate the converter between 48 and 42 V also increase. Thereby, higher switching losses in the converter cannot be avoided. As a tradeoff between the two scenarios, the turns ratio was chosen to be 3.

D. ZCS Condition for the Primary Switches

The stored energy in the parallel capacitors brings about ZCS of the primary switches under all operating conditions. Thereby, it is necessary to ensure that sufficient energy is stored in them to allow the antiparallel body-diode conduction without consider-ably increasing the circulating current. This imposes a constraint on the characteristic impedance at resonance, and the condition is given by

$$Z_r < \frac{3 V_{in,min} R_{FL}}{n V_o} \quad (25)$$

where $V_{in,min}$ is the minimum source voltage and R_{FL} is the full-load resistance. Z_r is selected such that ZCS is perpetuated for source voltage variations from 48 V down to 42 V and load variations, while limiting the circulating current

$$D_{min} = 0.33 + \frac{2nI_{in} L_s f_s}{3V_o} + \frac{f_n}{\pi}\sin^{-1}\frac{nZ_r I_{in}}{6V_o} + f_n \sin^{-1}\frac{nZ_r I_{in}}{3V_o} \quad (26)$$

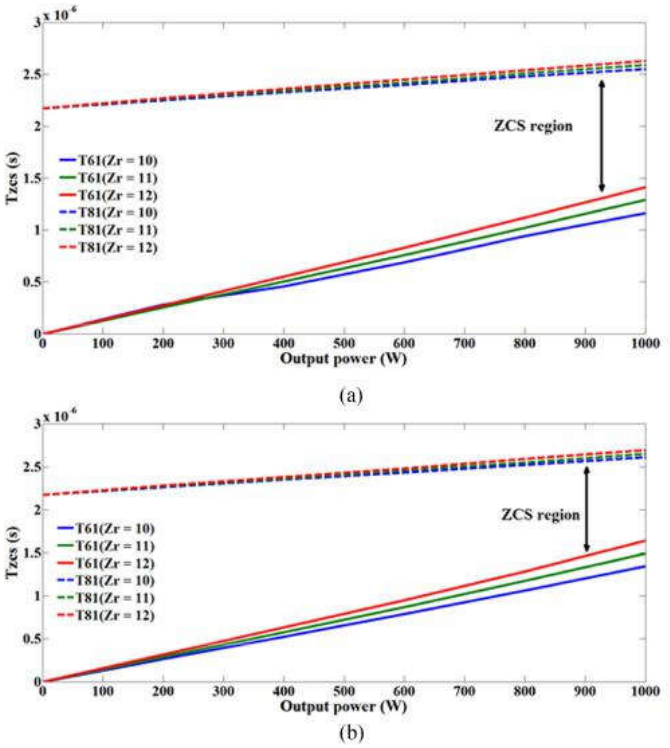


Fig. 5. ZCS region with load for (a) V_{in} = 48 V and (b) V_{in} = 42 V.

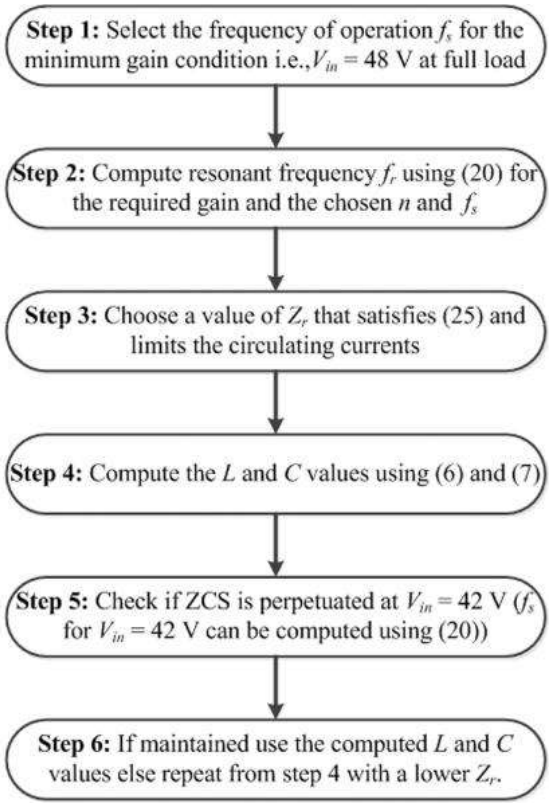


Fig. 6. Flowchart depicting the resonant tank design.

$$D_{max} = 0.33 + \frac{2nI_{in}L_s f_s}{3V_o} + \frac{f_n}{\pi}\sin^{-1}\frac{nZ_r I_{in}}{6V_o} + \frac{f_n}{2\pi}\sin^{-1}\frac{nZ_r I_{in}}{3V_o} + \frac{f_n}{2}. \quad (27)$$

E. Selection of Z_r

Z_r decides the circulating current through the circuit and, hence, the ZCS region at all power levels, as shown in Fig. 5. Lower Z_r widens the ZCS region by increasing the circulating current in the converter, as evident from Fig. 5. At rated power, narrow ZCS region of operation that ensures ZCS turn-off at 42 and 48 V is preferred to minimize the circulating currents. The ZCS region widens with load devaluation, and hence, ZCS operation is certain with load variations

Z_r > 11 Ω provides narrow ZCS operating region, while compromising on the voltage regulation with varying source voltage. Slightly lower Z_r of 11 Ω ensures strict voltage regulation with a slight increase in circulating current. Z_r < 11 Ω achieves the same by further increasing the circulating current, which is undesirable.

Hence, for perpetuating ZCS with limited circulating current and affirming strict voltage regulation under extreme source voltages, Z_r of 11 Ω was chosen. For Z_r = 11 Ω, the overlap period (T_{zcs}) is computed as 2.1 and 1.8 μs for V_{in} = 48 and 42 V, respectively, at rated power. From Fig. 5, T_{zcs} lies safely within the ZCS region. Hence, ZCS operation is certain with source voltage variations.

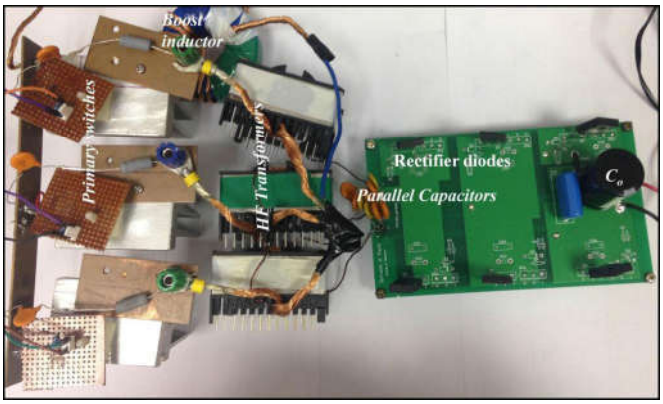


Fig. 7. Laboratory prototype of the proposed converter.

F. Resonant Tank Design

The design of the resonant tank parameters follows the flowchart shown in Fig. 6. In this example, the resonant frequency and the characteristic impedance are 0.2 MHz and 8.606, respectively, for V_{in} = 48 V at full load at 75 kHz. Thereby, the required values of L and C to perpetuate ZCS even at V_{in} = 42 V are 3 μH and 9 nF, respectively.

G. Duty Ratio

The minimum and maximum values of duty ratio within which the converter operates with ZCS are given by (26) and (27), respectively. The duty ratio D is selected such that D_{min}

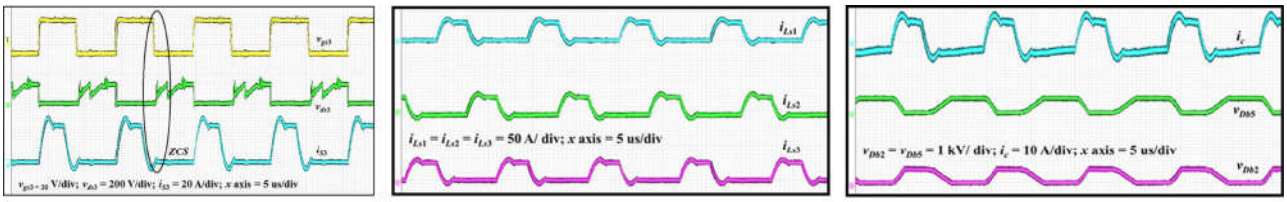


Fig. 8. Experimental results for V_{in} = 48 V, 1 kW at 95 kHz. (a) Gate-to-source voltage v_{gs3}, drain-to-source voltage v_{ds3}, and current i_{S3} through switch S_3. (b) Transformer primary currents i_{Ls1}, i_{Ls2}, and i_{Ls3} and (c) Secondary current i_c in phase C and voltage v_{Db2} and v_{Db5} across the rectifier diodes D_{b2} and D_{b5}.

TABLE IV
PARAMETERS OF THE LABORATORY PROTOTYPE

Components	Parameters
Boost inductors	MS250090 core, 12 turns, 52.2 μH
Primary switches	IPP110N20N3, 200 V, 88 A, $R_{ds,on}$ = 10.7 mΩ
Parallel capacitor	9 nF, 1 kV, ceramic capacitor
HF Transformers	three cores of N97 material, ETD 59 geometry, N_1 = 16, N_2 = 48, Leakage inductances referred to the primary L_{lk1} = 2.8 μH, L_{lk2} = 3 μH, and L_{lk3} = 3.1 μH
Output capacitors	100 μF, 400 V electrolytic and 2.2 μF, 400 V HF film capacitor
Rectifier diodes	STTH30R04, 400 V, 30 A, V_F = 0.97 V

$\leq D \leq D_{max}$ for all operating conditions to perpetuate ZCS for V_{in} = 42 to 48 V and from full-load to part-load conditions.

H. Boost Inductor Design

The value of the boost inductor L_b can be computed as

$$L_b = \frac{V_{Lb} - (T_{109} + T_{10})}{i} \quad (28)$$

where $V_{Lb} = V_{S1} - V_{Lm1} - V_{in}$ and $T_{10} = T_s/3 - (T_{32} + T_{63} + T_{86} + T_{109})$. The boost inductance was computed to be 132 μH for i = 0.05 A.

I. Body-Diode Conduction Time

The period the antiparallel body diode conducts ensuring ZCS is given by (18). The body-diode conduction dominates at light loads, as evident from (18), as the ratio of I_p/I_{in} elevates with load devaluation.

IV. EXPERIMENTAL RESULTS

This section details the experimental results to assess the converter's performance. Initially, the theoretical design was verified using PSIM 9.3.3. The simulation results can be found in [25]. Next, the proof-of-concept laboratory prototype shown in Fig. 7 was tested. Details of the prototype rated at 1 kW are provided in Table IV.

The gating signals to the primary switches were generated using Altera cyclone IV DE0-Nano. Semikron driver SKHI61R was used for driving the MOSFETs in the primary side. Fig. 8 depicts the experimental results obtained for V_{in} = 48 V at 1 kW, with the frequency of operation being 95 kHz. The input current I_{in} flows through the boost inductor with the ripple frequency $3 \times f_s$. Fig. 8(a) depicts the ZCS operation of the primary switching devices. The body diode of the switch takes over the switch current, thereby reducing the current through the switch to zero when the gating signal to it is removed. This eliminates the turn-off losses as the voltage across the switches shoots up to V_o/n when there is no current through the primary devices.

The commutation occurs when the gating signals of two switches overlap. During the device commutation, resonance sets in, transferring the current form the outgoing to the incom-ing phase. The resonance shapes the switch current waveform sinusoidally, as evident from Fig. 8(a).

The additional current required for the body-diode conduction is provided by the external capacitors in the circuit. The commutation of S_1 and S_2 takes place after 120° and 240°, respectively. Fig. 8(b) depicts the currents in the primary of the HF transformers. It is to be noted that the required leakage induc-tance in the path has been incorporated within the transformer itself. The transformer primary currents are indistinguishable from the switch currents and are phase shifted from one another by 120°.

Finally, Fig. 8(c) depicts the secondary current i_c through phase C and the voltage across the rectifier diodes D_{b2} and D_{b5}. It is evident that when the phase C current becomes posi-tive, the rectifier diode D_{b5} gets forward biased allowing power transfer to the load. The negative portion of the secondary phase current is the transformer magnetizing current. The transformer corresponding to phase C stores energy in the magnetizing in-ductance, thereby acting like a fly-back transformer.

The magnetizing current ripple is to be kept as low as possi-ble, as this decides the transformer core losses. This translates into higher magnetizing inductance for reducing the core losses and improving the conversion efficiency. The voltages across the rectifier diodes are free from ringing, as the voltages are clamped to the load voltage by the capacitive output filter C_o. This eliminates the need for additional snubbers in the sec-ondary. Additionally, the rectifier diodes also turn-off with zero current, eliminating reverse recovery issues due to the gradually decreasing current with a smaller slope.

The same has been illustrated for: 1) V_{in} = 48 V at 200 W and 2) V_{in} = 42 V at 1 kW in Figs. 9 and 10, respectively. The parallel capacitor voltage swinging between V_o and $-V_o$ is highlighted in Fig. 9(c). The experimental results match closely with the steady-state operating waveforms in Fig. 3. No discrepancies between them was observed. Furthermore, the results elucidate

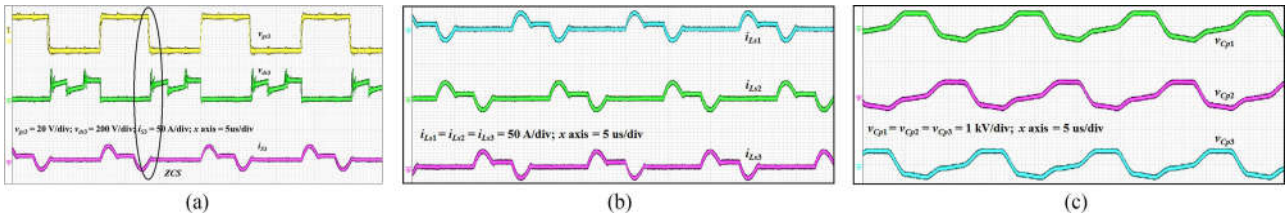


Fig. 9. Experimental results for V_{in} = 48 V, 200 W at 75 kHz. (a) Gate-to-source voltage v_{gs3}, drain-to-source voltage v_{ds3} S_3. (b) and current i_{S3} through switch Transformer primary currents i_{Ls1}, i_{Ls2}, and i_{Ls3} and (c) Voltage across the parallel capacitors v_{Cp1}, v_{Cp2}, and v_{Cp3}.

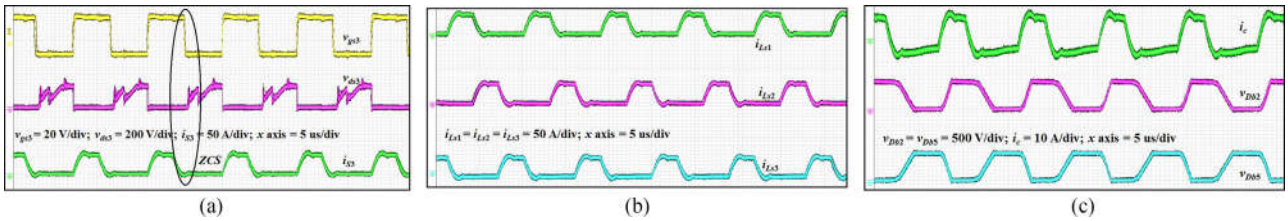


Fig. 10. Experimental results for V_{in} = 42 V, 1 kW at 112 kHz. (a) Gate to source voltage v_{gs3}, drain to source voltage v_{ds} and current i_{S3} through switch 3 S_3, (b) Transformer primary currents i_{Ls1}, i_{Ls2} and i_{Ls3} and (c) Secondary current i_c in phase C and voltage v_{Db2} across the rectifier diodes D_{b2} and v_{Db5} and D_{b5}.

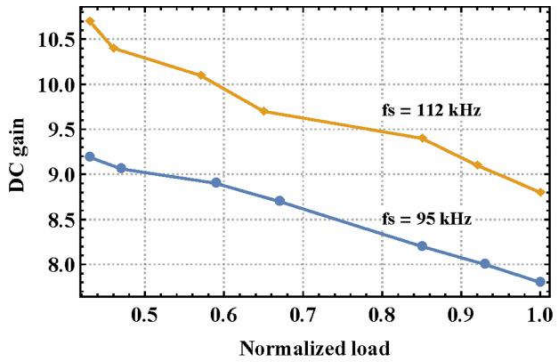


Fig. 11. Plot of the normalized load current versus the dc voltage gain.

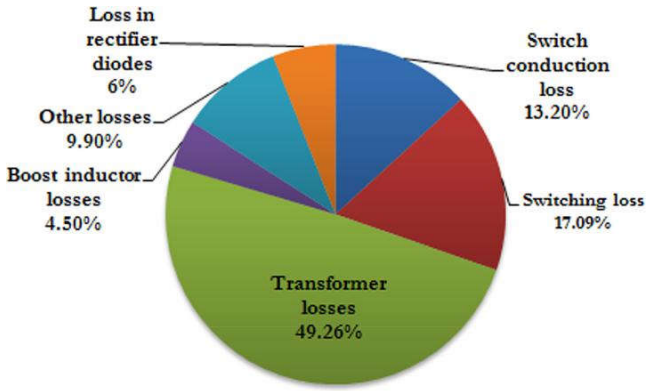


Fig. 12. Loss distribution in the converter for V_{in} = 48 V at full load.

the ZCS operation of the semiconductor devices and the device voltage clamping.

Frequency modulation ensures load voltage regulation and ZCS with natural voltage clamping under all operating conditions. Finally, the variation in the dc voltage gain with load for f_s = 95 and 112 kHz is shown in Fig. 11. This characteristic curve of the converter affirms the need for frequency variation to regulate the output voltage with load and input voltage variations. Maximum efficiency obtained was 92% at V_{in} = 48 V at full load. The loss distribution for V_{in} = 48 V at full-load condition is shown in Fig. 12.

The HF transformers contribute to 49.26% of the losses, as can be seen in Fig. 12. This accounts for approximately 40 W. With unidirectional core excitation, introduction of air gap in the transformers was necessary to avoid core saturation. Practically, with air gap, L_m dropped to 290 μH, although cores with higher cross-sectional area and large turns were deployed. Owing to low L_m, B remained sufficiently high, leading to higher core losses. The core losses of the transformer remain high even at light loads with slight variations in frequency. This depreciates the part-load efficiency drastically. The transformer utilization and the conversion efficiency can be improved by employing a single three-phase transformer. In such a configuration, the core excitation becomes bidirectional owing to flux cancellation. The net flux in the transformer at any instant is zero.

V. CONCLUSION

This paper focuses and investigates extending and implementing the concept of impulse commutation to a three-phase push–pull current-fed topology with a single inductor. Detailed operation, analysis, and design of this topology have been presented with impulse commutation. Soft commutation and voltage clamping of devices through impulse commutation have been demonstrated. It appears to be a strong concept for current-fed circuits and introduces a new class of unidirectional current-fed topologies. The operation is load adaptive to realize the merits at fixed source voltage. Impulse-commutated circuits are immune to load variation, so the control is simple to regulate the load voltage. Unlike resonant converters, impulse-commutation circuit introduces a short resonance and so limits the peak and circulating currents compared to resonant converters. Partial

resonance realizes soft commutation of devices, while keeping the circulating current low. With source variability, impulse commutation is maintained through variable-frequency modulation. With low peak and circulating currents through the devices, the strategy proves to be cost effective and efficient when compared to active clamping or passive snubbing.

REFERENCES

[1] A. K. Rathore and U. R. Prasanna, "Comparison of soft-switching voltage-fed and current-fed bi-directional isolated dc/dc converters for fuel cell vehicles," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2012, pp. 3212–3219.

[2] E. H. Kim and B. H. Kwon, "High step-up resonant push-pull converter with high efficiency," *IET Power Electron.*, vol. 2, no. 1, pp. 79–89, Jan. 2009.

[3] S.-K. Han, H.-K. Yoon, G.-W. Moon, M.-J. Youn, Y.-H. Kim, and K.-H. Lee, "A new active clamping zero-voltage switching PWM current-fed half-bridge converter," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1271–1279, Nov. 2005.

[4] P. J. Wolfs, "A current-sourced dc-dc converter derived via the duality principle from the half-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 40, no. 1, pp. 139–144, Feb. 1993.

[5] T. F. Wu, Y. C. Chen, J. G. Yang, and C. L. Kuo, "Isolated bidirectional full-bridge DC/DC converter with a flyback snubber," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1915–1922, Jul. 2010.

[6] S. Lee, J. Park, and S. Choi, "A three-phase current-fed push-pull dc-dc converter with active clamp for fuel cell applications," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2266–2277, Aug. 2011.

[7] P. Xuewei and A. K. Rathore, "Naturally clamped zero-current commutated soft-switching current-fed push-pull dc/dc converter: Analysis, design, and experimental results," *IEEE Trans. Power. Electron.*, vol. 30, no. 3, pp. 1318–1327, Mar. 2015.

[8] H. Cha, J. Choi, and P. Enjeti, "A three-phase current-fed dc/dc converter with active clamp for low-dc renewable energy sources," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2784–2793, Nov. 2008.

[9] H. Cha, J. Choi, and B.-M. Han, "A new three-phase interleaved isolated boost converter with active clamp for fuel cells," in *Proc. Power Electron. Spec. Conf.*, Jun. 2008, pp. 1271–1276.

[10] S. Oliveira and I. Barbi, "A three-phase step-up dc-dc converter with a three-phase high frequency transformer for DC renewable power source applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3567–3580, Aug. 2011.

[11] S. Bal and A. K. Rathore, "Modular snubberless bidirectional soft-switching current-fed dual 6-pack (CFD6P) DC/DC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 519–523, Feb. 2015.

[12] Y. Song *et al.*, "A current-fed three-phase half-bridge dc-dc converter with active clamping," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 1362–1366.

[13] P. Xuewei, U. R. Prasanna, and A. K. Rathore, "Magnetizing-inductance-assisted extended range soft-switching three-phase AC-link current-fed DC/DC converter for low DC voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3317–3328, Jul. 2013.

[14] R. Andersen and I. Barbi, "A three-phase current-fed push-pull dc-dc converter," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 358–368, Feb. 2009.

[15] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three phase soft-switched high-power-density dc/dc converter for high power applications," *IEEE Trans. Power. Electron.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[16] C. F. Chaung, C. T. Pan, and H. C. Cheng, "A novel transformerless interleaved four-phase step-down dc converter with low switch voltage and automatic uniform current-sharing characteristics," *IEEE Trans.Power. Electron.*, vol. 31, no. 1, pp. 406–417, Jan. 2016.

[17] D. S. Oliveira and I. Barbi, "A three-phase ZVS PWM DC/DC converter with asymmetric duty cycle for high power applications," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 370–377, Mar. 2005.

[18] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, design and experimental results of wide range ZVS active clamped L-L type current-fed dc-dc converter for fuel cells to utility interface: Analysis, design and experimental results," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 473–485, Jan. 2012.

[19] M. Ishibashi, M. Nakaoka, and Y. Konishi, "Performance evaluations of three-phase current-fed soft switching PWM converter with switched capacitor-type quasi-resonant snubber," *Proc. IEE—Electric Power Appl.*, vol. 148, no. 5, pp. 431–437, Sep. 2001.

[20] P. Xuewei and A. K. Rathore, "Naturally clamped soft-switching current-fed three-phase bidirectional DC/DC converter," *IEEE Trans. Ind. Elec-tron.*, vol. 62, no. 5, pp. 3316–3324, May 2015.

[21] K. R. Sree and A. K. Rathore, "Impulse commutated zero current switch-ing current-fed three-phase DC/DC converter," *IEEE Trans. Ind. Appl.*, vol. 52. no. 2, pp. 1855–1864, Mar. 2016.

[22] K. R. Sree and A. K. Rathore, "Impulse commutated zero current switch-ing current-fed push-pull converter: Analysis, design and experimen-tal results," *IEEE Trans. Ind. Electron.*, vol. 632, no. 1, pp. 363–370, Jan. 2015.

[23] R.-Y. Chen, T.-J. Liang, J.-F. Chen, R.-L. Lin, and K.-C. Tseng, "Study and implementation of a current-fed full-bridge boost DC-DC converter with zero-current switching for high-voltage applications," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1218–1226, Jul./Aug. 2008.

[24] N. Yuan, X. Yang, X. Zeng, J. Duan, J. Zhai, and L. Donghao, "Analysis and design of a high step-up current-fed multiresonant DC-DC converter with low circulating energy and zero-current switching for all active switches," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 964–978, Feb. 2012.

[25] R. S. K. Moorthy and A. K. Rathore, "Analysis and design of impulse commutated ZCS three-phase current-fed push-pull DC/DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Exp.*, Long beach, CA, USA, Mar. 2016, pp. 794–801.