Performance Analysis of DC – DC converters with voltage-lift Circuits

G. Jegadeeswari[1], V. Vanisree[2], S. Janarthanan[3]

Assistant Professor[1,3], Department of EEE, AMET Deemed to be University, Chennai, India.

Assistant Professor[2], Department of EEE, Shri Krishnaa Colg of Engg & Tech, Pondicherry, India

E-mail: jegadeeswari.dharan@gmail.com[1], vanisree.eee@gmail.com [2] , s.janarthanan@ametuniv.ac.in[3]

Abstract

The voltage-lift circuit has been successfully applied to several series of DC-DC converters. However, the voltage-lift circuit definitely has an unavoidable influence on the overall converter performance. It is attempted to clarify such an effect. Four converters with voltage-lift circuit are analysed: positive output self-lift converter, positive output super-lift converter, negative output self-lift converter and positive output re-lift converter. It is assumed that these converters operate in both continuous and discontinuous conduction modes. The converter performance in continuous conduction mode is first analysed. The boundary between continuous and discontinuous conduction modes and the modified voltage transfer gain are derived for each circuit. In addition, formulas for calculating the filling efficiency in DCM for the four converters are given. Both the simulation and experimental results verify the theoretical analysis.

Key Words: DC-DC Boost Converter, Voltage Lift Technique, Positive output super Lift Technique

1 INTRODUCTION

DC-DC converters are electronic devices used whenever we want to change DC electrical power efficiently from one voltage level to another. They are needed because unlike AC, DC can't simply be stepped up or down using a transformer. In many ways, a DC-DC converter is the DC equivalent of a transformer. A DC-to-DC converter is a device that accepts a DC input voltage and produces a DC output voltage. Typically the output produced is at a different voltage level than the input. In addition, DC-to-DC converters are used to provide noise isolation, power bus regulation, etc. There are many different types of DC-DC converter, each of which tends to be more suitable for some types of application than for others. For convenience they can be classified into various groups, however. For example some converters are only suitable for stepping down the voltage, while others are only suitable for stepping it up; a third group can be used for either [1]–[4].

A buck converter is a step-down DC-to-DC converter. Its design is similar to the step-up boost converter, and the boost converter is a switched-mode power supply that uses two switches and an inductor, and optionally a capacitor to buffer the output.

The boost converter converts an input voltage to a higher output voltage. It is also named the step-up converter. Boost converters are used in battery powered devices, where the electronic circuit requires a higher operating voltage than the battery can supply, e.g. notebooks, mobile phones and camera flashes [5]-[6].

The fly back converters tend to be used for relatively low power applications like generating high voltages for insulation testers, Geiger counter tubes, cathode ray tubes and similar devices drawing relatively low current. Typical applications of DC-DC converters are where 24V DC from a truck battery must be stepped down to 12V DC from a car battery must be stepped down to 3V DC, to run a personal CD player; where 5V DC on a personal computer motherboard must be stepped down to 3V, 2V or less for one of the latest CPU chips; where the 340V DC obtained by rectifying [7]-[9].

Boost converters are made of a simple structure and cheap topology. These converters have superior performance in terms of high voltage gain and minimum output ripple. The converters are developed based on two techniques, the voltage-lift technique and the super-lift technique [10].

Series DC–DC Boost converters have been successfully implemented with the voltage-lift technique, which results in good performance such as high voltage transfer gain (VTG) and low ripple voltage and current. Positive output Boost converters, negative output Boost converters and positive output super-lift converters were proposed. Especially for the positive output super-lift converter, the VTG will increase according to a power law when the converter is used for cascade connection, which needs further consideration for future application. The voltage-lift circuit (VLC) has been applied in each circuit of these DC–DC converters except for the elementary circuits of positive and negative output Boost converters.

Although the application of VLCs gives a high VTG in Boost converters, VLCs may also bring some undesired problems. For example, the output voltage of the Boost converters will be affected by the capacitor in the VLC. Small load resistance, which causes the currents in the circuit to increase, will augment the influence of VLC on the converter's VTG. VLCs also affect the boundary of the converters between the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) and the filling efficiency in DCM. At present, the above-mentioned effects of the VLC still remain unclear.

The rest of the paper is divided into four sections. The converter design and simulation is explained in Section 2. hardware implementation is presented in Section 3. Finally we conclude with Section 4.

2. CONVERTER DESIGN AND SIMULATION

2.1 TOPOLOGIES

Combining both the voltage-lift and super-lift techniques, there are many topologies are available and they are categorized based on the techniques upon which it is implemented and the number of stages it is used. In this paper the following topologies from the voltage-lift and super-lift converter are analyzed.

- Positive Output Self-Lift converter (POSLC)
- Negative Output Self-Lift Converter (NOSLC)
- Positive Output Re-lift converter (PORLC)
- Positive Output Super-lift converter (POSC)

The POSLL, PORL, NOSLL are the Boost converter developed on the voltage lift techniques and the POSL is an Positive Output Super-lift Boost Converter using the Super-Lift Technique. Based on the Number of the stages used in the converter circuit, they are named as Re-lift for two stages, Triple-lift for three stages, and Quadruple-lift for four stages of the lifting circuits. The design and simulated results of the above mentioned topologies are discussed below.

2.2 POSITIVE OUTPUT SELF-LIFT CONVERTER (POSLC)

The self-lift circuit is similar to the elementary circuit, only it has another capacitor and diode added to the pump circuit to provide greater lift. Capacitor C1 is in the circuit to raise the voltage across capacitor C by Vi (source voltage), and consequently raise the output voltage. This means that the self-lift is unable to provide a step-down output.

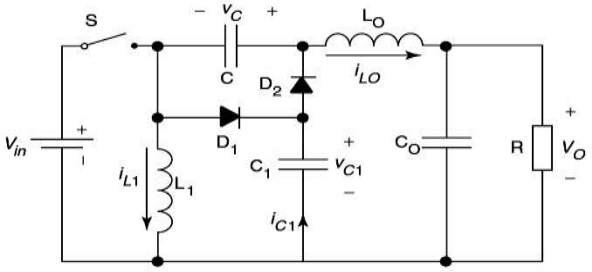
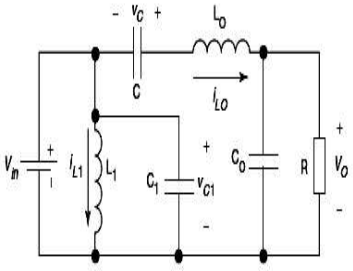


Fig 2.1 Positive output self-lift boost converter

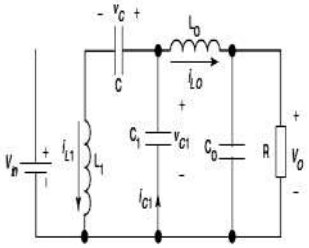
2.2.1 POSL converter circuit analysis in CCM

The inductor (L1) current increases in the switch-on period and decreases in the switch-off period. The corresponding voltage across L1 is Vin and VL1-off.



switch-on condition

Fig 2.2 POSL converter



switch-off condition

Fig 2.3 POSL

Therefore,

$K\ T\ V_{in} = (1-k)\ T\ (V_{L1\text{-}off})$ --- (2.1)

$V_{L1\text{-}off} = K\ /\ (1-K)V_{in}$ --- (2.2)

During switch-on period, the output voltage is equal to Vin plus the voltage across C. Therefore,

$Vo = V_{in} + Vc$ --- (2.3)

$Vc = V_{c\text{-}off} = V_{L1\text{-}off}$ --- (2.4)

$= k / (1-K)V_{in}$ --- (2.5)

$Vo = k / (1-K)\ V_{in} + V_{in}$ --- (2.6)

$= 1/(1-K)\ V_{in}$ --- (2.7)

The ideal voltage transfer gain,

$M = Vo / V_{in} = 1 / (1-K)$ --- (2.8)

2.2.2 POSL converter circuit analysis in DCM

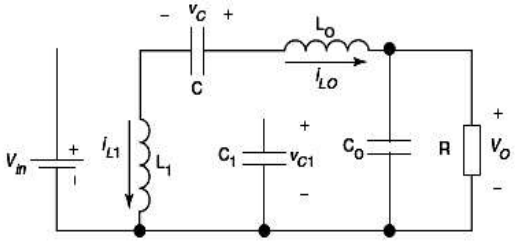


Fig 2.4 POSL converter in DCM

When the circuit operates in DCM, during switch-off, the current flowing through the diode D2 reaches zero at time t1 before the next switch-on period. The filling efficiency, can be defined as

$$\xi = \frac{t_1 - kT}{(1-k)T}$$ --- (2.9)

It means that after ξ(1–k)T from switch-off instant, the current flowing through diode D2 is zero. the expression of the filling efficiency ξ can be derived as

$$\xi = \frac{1 + \sqrt{1 + 4\lambda_1 k^2 Z_N}}{2\lambda_1 k(1-k)Z_N}$$ --- (2.10)

Let ξ =1; the boundary condition between the CCM and DCM is derived as

$$Z_N \lambda_1 k(1-k)^2 = 1$$ --- (2.11)

2.2.3 Simulation results

In the simulations and experiments, the circuit parameters are: Vin=20V, L1=L2=1mH, C1=2.2uf, c = co = 20uf and k=0.3. The switching frequency is 20KHz. When ξ =1, the circuit is under critical DCM, the value of R=124.7Ω. Figure shows the simulation circuit and the waveforms of the POSLL converter under the critical DCM.

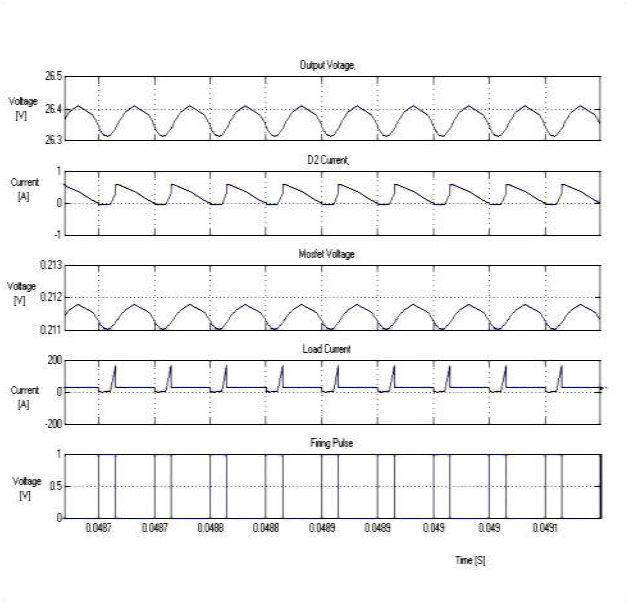


Fig 2.5 POSL Converter output response

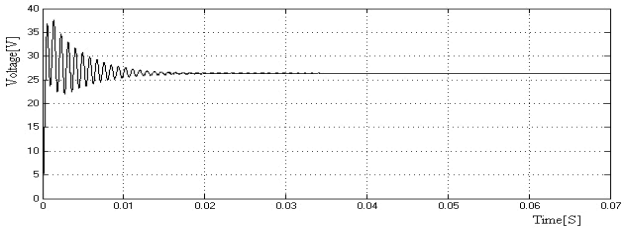


Fig 2.6 POSL Converter voltage response

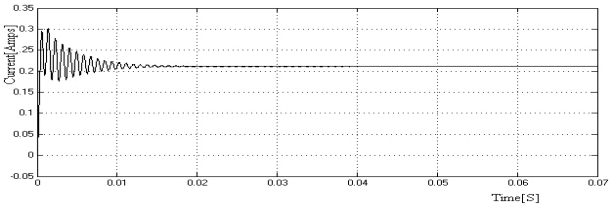


Fig 2.7 POSL converter current response

2.3 NEGATIVE OUTPUT SELF-LIFT CONVERTER (NOSLC)

The Negative Output Self-lift Boost converter shown in the figure below is derived from the elementary circuit of negative output Boost converter. The VLC in the Figure consists of capacitor C1 and diode D1. Capacitor C is the pump capacitor. The two inductors L1 and LO are of the same inductance. Figure 4.2 shows the equivalent circuits of the NOSLL converter in various states

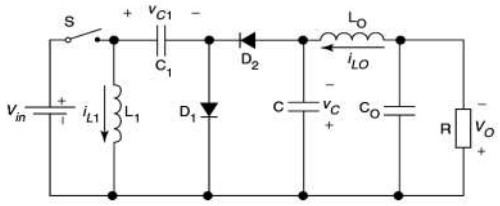


Fig 2.8 Negative output self-lift boost converter

2.3.1 NOSL converter circuit analysis in CCM

The inductor (L1) current increases in the switch-on period and decreases in the switch-off period. The voltage balance of the inductor (L1) is given by

$$K\ T\ Vin = (1-k)T(V_{L1\text{-}off}) \quad \text{--- (2.12)}$$

$$V_{L1\text{-}off} = K / (1-K)\ Vin \quad \text{--- (2.13)}$$

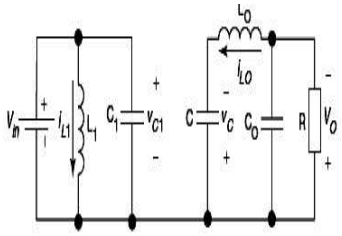


Fig 2.9 NOSL converter switch-off condition

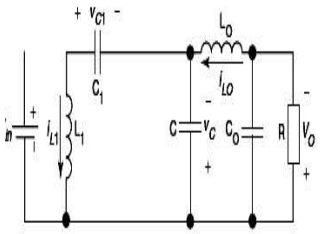


Fig 2.10 NOSL converter switch-on condition

During switch-on period, the output voltage is equal to the voltage across capacitor C. Therefore, Vo = Vc

$$Vc = V_{c\text{-}off} = V_{L1\text{-}off} + Vc1 \quad \text{--- (2.14)}$$

$$= k/(1-K)Vin + Vin \quad \text{--- (2.15)}$$

$$= 1/(1-K)\ Vin \quad \text{--- (2.16)}$$

The ideal voltage transfer gain ,

$$M = Vo / Vin = 1/(1-K) \quad \text{--- (4.17)}$$

2.3.2 NOSL converter circuit analysis in DCM

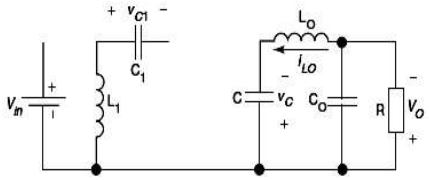


Fig 2.11 NOSL converter in DCM

The DCM of the NOSSL converter means that the inductor current iL1 reaches zero during switch-off period before the next switch-on period. Define the time when iL1 reaches zero as t1; the filling efficiency ξ is given by

$$\xi = \frac{t_1 - kT}{(1-k)T} \quad \text{--- (2.18)}$$

The filling efficiency ξ can be derived as

$$\xi = \frac{1 + \sqrt{1 + 2\lambda_1 Z_N k^2}}{\lambda_1 Z_N k(1-k)} \quad \text{--- (2.19)}$$

Let ξ=1; the boundary condition between CCM and DCM is derived as

$$\lambda_1 Z_N k(1-k)^2 = 2 \quad \text{--- (2.20)}$$

2.3.3 Simulation results

The circuit parameters for simulations and experiments are: vin=20V, L1=L0=1mH, C1=2.2uf, c = co = 20uf and k=0.3. The switching frequency is 20KHz. When ξ =1, the circuit is under critical DCM, the value of R=260.7Ω. Figure shows the simulation circuit and the waveforms of the NOSLL converter under the critical DCM.

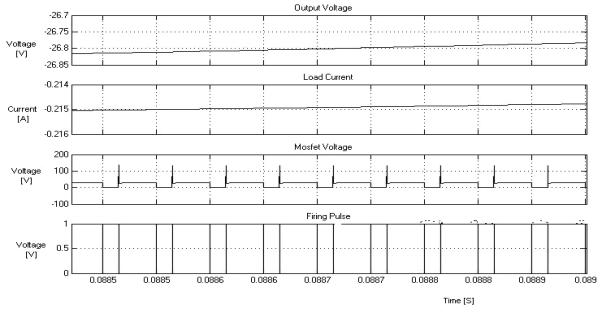


Fig 2.12 Output responses of NOSL converter

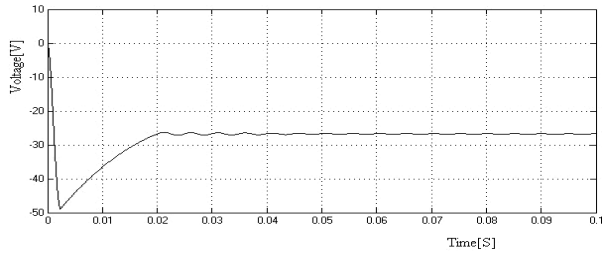


Fig 2.13 Voltage response of NOSL converter

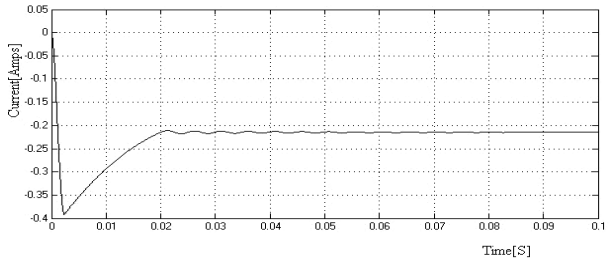


Fig 2.14 Current response of NOSL converter

2.4 POSITIVE OUTPUT RE-LIFT BOOST CONVERTER (PORLC)

The positive output re-lift Boost (PORLL) converter has two voltage lift circuits and the converter is shown in Fig.4.5. Compared with the POSLL converter, an extra VLC, which consists of a capacitor C2 and a diode D2, is added to the circuit. Another switch S1 is implemented, as shown in the Figure. It is turned on and off at the same time as the switch S. Two capacitors, C1 and C2, are the same. The selection of inductance will be discussed later.

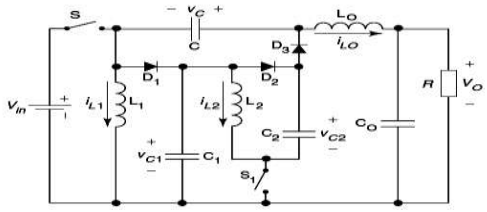


Fig 2.15 Positive output re-lift boost Converter

2.4.1 PORL converter circuit analysis in CCM

The inductors (L1& L2) current increases in the switch-on period and decreases in the switch-off period. The voltage balance for the inductors are,

$K\ T\ Vin = (1-k)\ T\ (V_{L1\text{-}off})$ --- (4.21) $V_{L1\text{-}off} = K / (1-K)\ V_{in}$ --- (4.22)

$V_{L2\text{-}off} = K / (1-K)\ Vin$ --- (2.23)

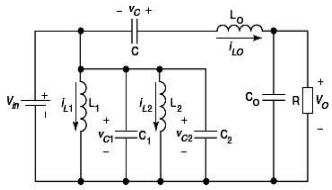


Fig 2.16 PORL converter

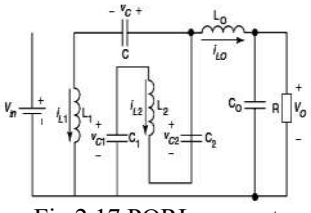


Fig 2.17 PORL converter switch-on condition

switch-off condition

During switch-on period, the output voltage,

$Vo = Vin + Vc$ --- (2.24)

$Vc = V_{c\text{-}off} = V_{L1\text{-}off} + V_{L2\text{-}off} + Vc1 + Vc2$ -- (2.25)

$= k / (1-K)Vin + k / (1-K)Vin + Vin + Vin$ --- (2.26)

$= 2k / (1-K)Vin + 2Vin$ --- (2.27)

$$Vc = 2 / (1-K)\ Vin \quad \text{--- (2.28)}$$

$$Vo = 2 / (1-K)\ Vin + Vin \quad \text{--- (2.29)}$$

$$= Vin*2 / (1-k) \quad \text{---(2.30)}$$

The ideal voltage transfer gain,

$$M = Vo / Vin = 2 / (1-K) \quad \text{--- (2.31)}$$

2.4.2 PORL converter circuit analysis in DCM

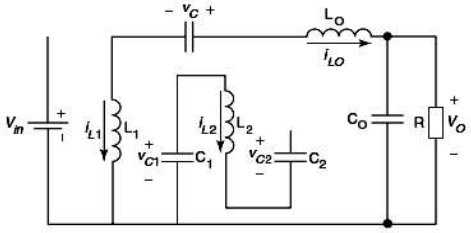


Fig 2.18 PORL converter in DCM

The DCM of the PORLL converter means that the Diode current D3 reaches zero during switch-off period before the next switch-on period. Define the time when iL1 reaches zero as t1; the filling efficiency ξ is given by

$$\xi = \frac{t_1 - kT}{(1-k)T} \quad \text{--- (2.32)}$$

The filling efficiency ξ can be derived as

$$\xi = \frac{2 + \sqrt{4 + 4\lambda_2 Z_N k^2}}{\lambda_2 Z_N k(1-k)} \quad \text{--- (2.33)}$$

2.4.3 Simulation results

The circuit parameters for simulations and experiments are: vin=20V, L1=L0=1mH, L2 = 0.5mH, C1=C2=2.2uf, c = co = 20uf and k=0.3. The switching frequency is 20KHz. When ξ =1, the circuit is under critical DCM, the value of R=249.4Ω. Figure shows the simulation circuit and the waveforms of the PORLL converter under the critical DCM.

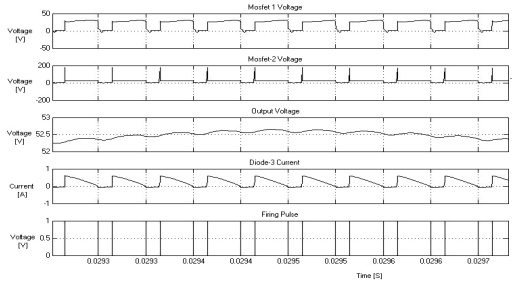


Fig 2.19 Output responses of PORL converter

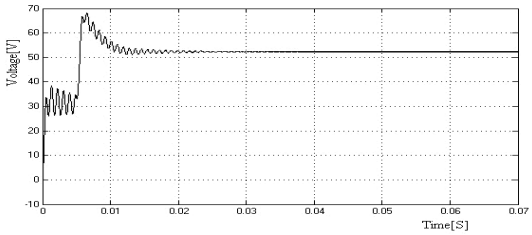


Fig 2.20 Voltage response of PORL converter

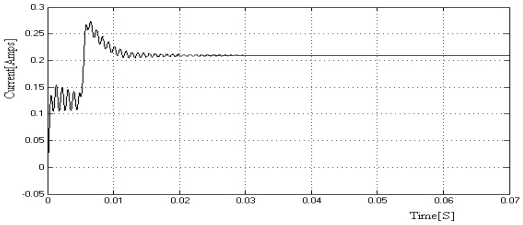


Fig 2.21 Current response of PORL converter

2.5 POSITIVE OUTPUT SUPER-LIFT CONVERTER (POSLC)

The positive output super-lift (POSL) converter is a newly derived DC–DC converter, which is shown in Fig.4.8. The converter has one VLC, which includes the diode D1and the capacitor C1. During switch-on period, the voltage VC1 across C1 increases to Vin in a short time. At this moment the diode D2 will be blocked and iD2 = 0. The output current is io=vo=R. During switch-off period, the inductor current iL1 flows through C1, D2 and the output port. Thus, iL1=iD2=io

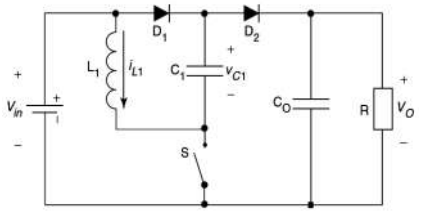


Fig 2.22 Positive output super-lift boost converter

2.5.1 POSL converter circuit analysis in CCM

The inductor (L1) current increases in the switch-on period and decreases in the switch-off period. The voltage balance for the inductor is,

$$K\ T\ Vin = (1-k)\ T\ (V_{L1\text{-}off}) \quad \text{--- (2.34)}$$

$$V_{L1\text{-}off} = K / (1-K)Vin \quad \text{--- (2.35)}$$

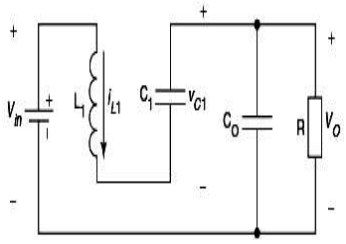


Fig 2.24 POSL converter switch-on condition

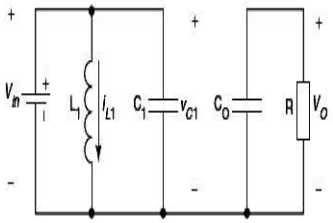


Fig 2.23 POSL converter switch-off condition

During switch-off period, the output voltage ,

$$Vo = Vin + Vc1 + VL1 \quad \text{--- (2.36)}$$

$$= Vin + Vin + V_{L1\text{-}off} \quad \text{--- (2.37)}$$

$$= Vin + Vin + k / (1-K)\ Vin \quad \text{--- (2.38)}$$

$$Vo = Vin\ (2-k) / (1-K) \quad \text{--- (2.39)}$$

The ideal voltage transfer gain,

$$M = Vo/Vin = (2-k) / (1-K) \quad \text{--- (2.40)}$$

2.5.2 POSL converter circuit analysis in DCM

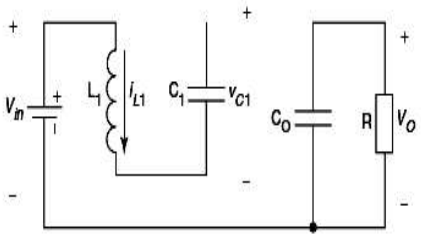


Fig 2.25 POSL converter in DCM

The DCM of the NOSSL converter means that the inductor current iL1 reaches zero during switch-off period before the next switch-on period. Define the time when iL1 reaches zero as t1; the filling efficiency ξ is given by

$$\xi = \frac{t_1 - kT}{(1-k)T} \quad \text{--- (2.41)}$$

the filling efficiency ξ can be derived as

$$\xi = \frac{2 + \sqrt{4 + 2\lambda_1 Z_N k^2}}{\lambda_1 Z_N k(1-k)} \quad \text{--- (2.42)}$$

2.5.3 Simulation results

The circuit parameters for simulations and experiments are: vin=20V, L1=1mH, C1=2.2uf, Co = 20uf and k=0.3. The switching frequency is 20KHz. When ξ =1, the circuit is under critical DCM, the value of R=451.2Ω. Figure shows the simulation circuit and the waveforms of the POSL converter under the critical DCM.

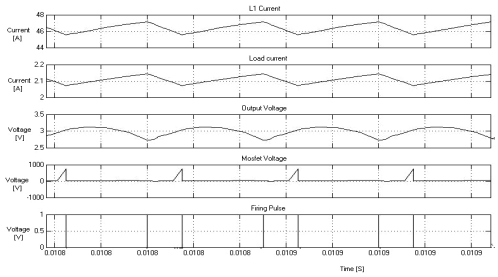


Fig 2.26 Output responses of POSL converter

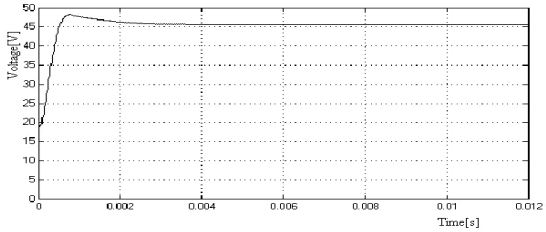


Fig 2.27 Voltage response of POSL converter

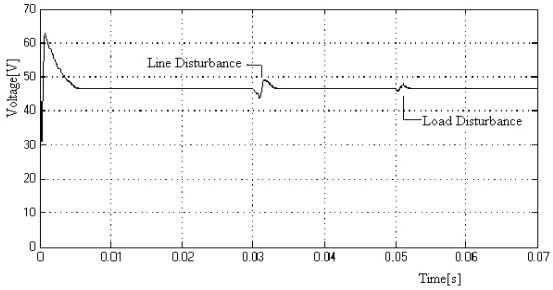


Fig 2.28 Voltage response of POSL converter for line and load disturbance for 1msec

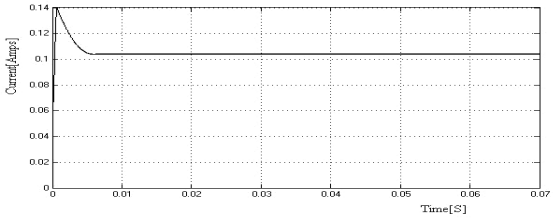


Fig 2.29 Current response of POSL converter

3. HARDWARE IMPLEMENTATION

A boost converter (step-up converter) is a power converter with an output dc voltage greater than its input dc voltage. It is a class of switching mode power supply (SMPS) containing at least two semiconductor switches and at least one energy storage element. Filters made of inductor and capacitor combinations are often added to a converter's output to improve performance. All the voltage lift techniques were analyzed and simulated. From the various techniques, the super lift technique has the better voltage transfer gain and cheaper topology when compared to other topologies and the super lift Boost converter is implemented in hardware.

3.1 CALCULATION OF CIRCUIT PARAMETERS

The circuit parameters were calculated such that the circuit will operate in the critical DCM. So, that the filling efficiency ξ=1. The boundary condition between CCM and DCM is

$$\frac{\lambda_1 Z_N k(1-k)^2}{2(2-k)} \geq 1 \quad \text{--- (3.1)}$$

The normalized load for POSL converter is

$$Z_N = R/fL_1 \quad \text{--- (3.2)}$$

The VLC coefficient λ1 has an influence on the ideal VTG of the circuit.

$$M_{POSL} = \frac{1}{\lambda_1}\frac{2-k}{1-k} \quad \text{---(3.3)}$$

$$\lambda_1 = \frac{\tilde{M}_{POSLL}}{M_{POSLL}} = 1 + \frac{1}{2RC_1 f} \quad \text{--- (3.4)}$$

The converter circuit will operate at DCM, when ξ< 1.The converter's gain will meet the ideal VTG, when filling efficiency λ1=1. From the boundary condition, the circuit parameters were calculated for K= 0.3, L1 = 1mH, C1 = 2.2μf, f = 20 KHz and R = 451.2Ω. The corresponding λ1 is 1.025.

For the proposed design the voltage transfer gain of the converter circuit is approximately equal to ideal gain,

M= (2-K)/ (1-K) --- (3.5)

Thus for input voltage of 20V at 0.3 duty ratio, the output of the converter is 47.4V

3.2 SPECIFICATIONS

- Mosfet – IRF540
- Diode – MBR6045WT
- Inductance – 1mH
- Capacitance- 2.2μf and 20μf
- Resistance - 50 to 500 ohms
- Pulse Generator – XR8038

3.3 TRIGERRING OF MOSFET

To give gate pulse to the mosfet there are more methods are there. Here using XR8038a is used to give gate pulse. The pulse from the pulse generator IC is given to a common emitter transistor driver circuit to drive the Mosfet. The transistor SL100, which is an NPN transistor, is used in the driver circuit. The MOSFET is triggered with a square pulse of 0.3 or 33% duty factor. When the duty factor is varied with in an allowable range the magnitude of the output voltage can be increased to a certain desired level.

- The frequency of switching for our converter is 20000Hz.
- The duty cycle of the wave is 30%.
- The value of frequency is 5*10^-5 s
- The ON time period is 1.5*10^-5 s
- The OFF time period is 3.5*10^-5 s

3.4 INDUCTOR DESIGN

Inductance (*L*, measured in henries) is an effect which results from the magnetic field that forms around a current-carrying conductor. Electrical current through the conductor creates a magnetic flux proportional to the current. A change in this current creates a change in magnetic flux that, in turn, generates an electromotive force (EMF) that acts to oppose this change in current. Inductance is a measure of the amount of EMF generated for a unit change in current. For example, an inductor with an inductance of 1 Henry produces an EMF of 1 volt when the current through the inductor changes at the rate of 1 ampere per second. The number of turns/loops, the size of each turn, and the material it is wrapped around all affect the inductance. For example, the magnetic flux linking these turns can be increased by coiling the conductor around a material with a high permeability [12]-[14].

3.4.1 Energy Stored

The energy (measured in joules, in SI) stored by an inductor is equal to the amount of work required to establish the current through the inductor, and therefore the magnetic field. This is given by:

$$E_{\text{stored}} = \frac{1}{2}LI^2 \quad \text{--- (3.6)}$$

Where L is inductance and I is the current flowing through the inductor.

3.4.2 Inductor Construction

An inductor is usually constructed as a coil of conducting material, typically copper wire, wrapped around a core either of air or of ferromagnetic material. Core materials with a higher permeability than air confine the magnetic field closely to the inductor; thereby increasing the inductance.The inductor for our hardware circuit was constructed as an air core inductor.
The design calculation for the inductor is shown below

$$L = \frac{D_a^{\,2} * T^2}{1000 * (18 * D_a + 40 * C_l)} \quad \text{--- (3.7)}$$

Da= Average Turn Diameter in inches
Cl= Coil Length in inches
T = Number of Turns
Based on the design calculation for an inductor is 1mH, by using the following parameters,
The length of the coil is 2.2cm (0.86inch)
The diameter of the coil is 2cm (0.78 inch)
Turns per level calculated,
No. of turns is 256.
Turns per level is 40
Gauge of wire used is 25SWG

3.5 COMPARISON OF OUTPUT VOLTAGES

The output voltage of the hardware and simulation are compared and verified to check the performance of the hardware by varying various factors affecting the output voltage of the circuit. The output voltages are tabulated below for each type variation separately. The same is also expressed as graphical notation.

3.5.1 Line Variation

The output voltage is verified with different input voltage by keeping the value of K and Duty ratio as constant (K=0.3, R_L= 451.2 ohms).

Table 3.1 Output response of POSL for Line variation

Input Voltage (Vin)	Simulation Output (Vout)	Hardware Output (Vout)
11	25.1	25.7
20	46.7	47.2
30	70.9	71.4

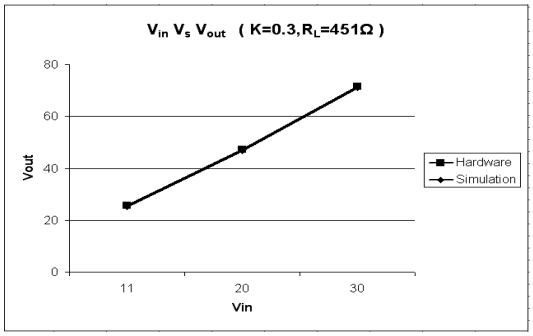


Fig 3.1 Output response of POSL for Line variation

3.5.2 Duty Variation

The output voltage is verified with different duty ratio by keeping the value of input voltage and the load resistance as constant (Vin = 20V, R_L = 451.2 ohms)

Table 3.2 Output response of POSL for Duty variation

Duty Cycle(K)	Simulation Output (Vout)	Hardware Output (Vout)
0.2	43.1	43.3
0.3	46.7	47
0.5	58.2	58.5

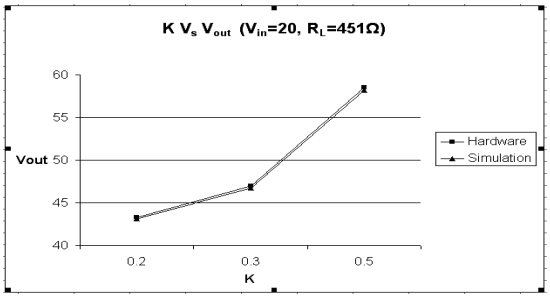


Fig 3.2 Output response of POSL for Duty variation

3.5.3 Load Variation

The output voltage is verified with different load by keeping the value of input voltage and the duty factor as constant (Vin = 20 V, K = 0.3)

Table 3.3 Output response of POSL for Load variation

Load Resistance (Ohm)	Simulation Output (Vout)	Hardware Output (Vout)
450	46.8	47.3
400	46.7	46.8
350	46.3	46.4

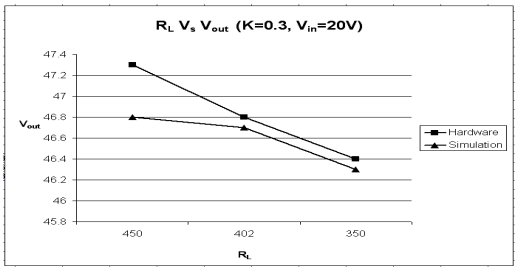


Fig 3.3 Output response of POSL for Duty variation

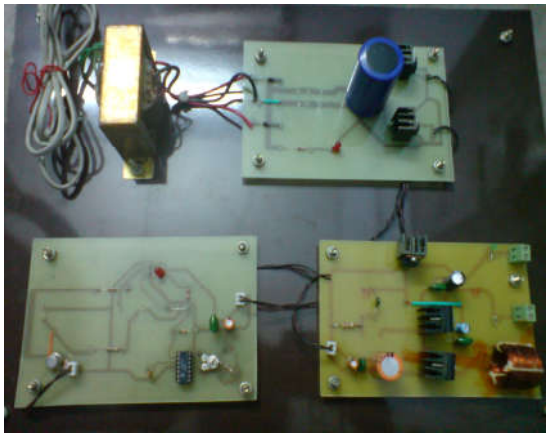


Fig 3.4 Completed hardware kit

4. CONCLUSION

Traditional DC-DC Boost converters are used in high voltage applications, but they are not economical due to the limited output voltage, efficiency and require complex control algorithm. Moreover due to the effect of parasitic elements the output voltage and power transfer efficiency of DC-DC converters are limited. These limitations are overcome by using the voltage lift technique. The voltage lift circuit is employed in the Boost converter; these converters perform DC-DC voltage conversion with high power density, high efficiency, low cost with simple structure, small ripples and wide range of control. Super-Lift technique is quite similar to the voltage-Lift technique in design. But Super-Lift technique has far superior gain than the voltage-lift technique. Due to its geometric gain of the Super-Lift Technique, there is huge potential for the Super-Lift Boost converters when comparing to converters using the Voltage-Lift technique. For this reason it is thought that no further development in the Voltage-Lift Technique ought to take place, and efforts are focused on the Super-Lift Technique. Super-Lift converter can achieve high gains while maintaining high efficiency and it could be applied to many current applications. The performance of POSL converter was studied for both line and load disturbances experimentally. The experimental results are verified with simulation result and it is found to be more identical with the simulation results. The components of the Super-lift converter are smaller and cheaper than Fly-back converters as there is no transformer, so there may be applications where the Super-Lift Boost converters are more feasible.

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