Optimal Location of Unified Power Flow Conditioner for Enhancing Power Transfer Capability in 14 Bus System

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Abstract

This paper addresses the optimal location of UPFC for maintaining magnitude of bus voltage and enhancing the power transfer capacity in 14 bus system. In this paper the improved double loop PI Control based approach is used for controlling the series and parallel converter of UPFC. This paper set up simulink model of UPFC in MATLAB/ Simulink environment under normal, load changing and fault condition in 14 bus system in both the case with and without UPFC .The simulation result show that this double loop based PI control strategy for UPFC can effectively control the voltage and power flow, maintain the bus voltage , Active power at different bus and reduce reactive exchange.

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Keywords: *UPFC, double loop PI control, 14 bus System, active power, reactive power.*

1. Introduction

Flexible AC transmissions devices have been extensively used to enhanced the power transfer capability & increase the amount of power flow through the transmission network and also reduce the line losses. FACTS Controllers are categorized into synchronous compensator, thyristor-controlled series capacitor, static VAR compensator (SVC), static SSSC and unified power flow controller (UPFC) [1]. UPFC is one of the most important facts device. Since, it can maintain all the network parameters such as system impedance, amplitude of voltage and angle. UPFC combines the features of many FACTS equipment. It controls magnitude of voltage, phase angle and power of line. The main objective of this is to improved the voltage stability and power flow control in power system network using Unified power flow controller [2]. For selection of optimal location many algorithms are available such as Optimal Power Flow, Evolutionary Programming, Harmony Search (HS), PSO , simulated annealing . For design of system only need steady state model many survey have already done on this.in this paper actual operation UPFC on standard IEEE-14 is described. Using UPFC voltage profile of network are improved and line losses are also reduces. Double loop based PI controller used as controller for series and shunt converter of UPFC. Section II described proposed methodology of system. Section III Mathematical modeling of UPFC. Section IV PI based double loop control of series and shunt control of UPFC. Section V includes the simulation results obtained MATLAB simulink and concluded by section VI.

2. Proposed Methodology

Basic model of unified power flow conditioner are shown in fig.1 UPFC consist shunt and series converter. Series converter connected in series with line through transformer. it inject the voltage in series with line. Shunt converter connected in parallel with line and inject the current in parallel with line. Closed loop PI based double loop control used to control the shunt and series converter. Voltage from the system is sense and compare with reference signal then it fed to PI controller it reduce the error output of this is fed to PWM generator which generate the pulses for Inverter.

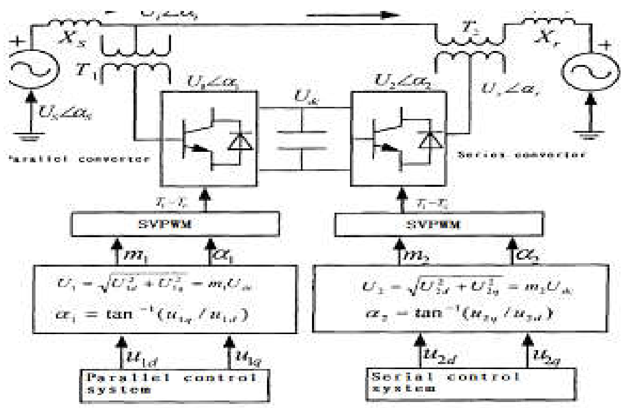

Figure 1. Basic Structure of UPFC connected to power system

3. Mathematical Modeling of UPFC.

Mathematical modeling of UPFC for two simple machine are given below. Using UPFC the power flow of line in terms of real and reactive power expressed as follow.

$$P\text{-}jQ = V_r\left(\frac{V_s+V_{pq}-V_r}{jX}\right) \qquad (1)$$

$$P\text{-}jQ = V_r\left(\frac{V_s-V_r}{jX}\right)^* \qquad (2)$$

Thus $V_{pq} \neq 0$, Net active and reactive power given in the form of

$$P\text{-}jQ = V_r\left(\frac{V_s-V_r}{jx}\right)^* + \frac{V_r V_{pq}^*}{-jx} \qquad (3)$$

Where,

$$V_s = Ve^{j\frac{\partial}{2}} = V\left(\cos\frac{\partial}{2} + j\sin\frac{\partial}{2}\right)$$

$$V_r = Ve^{-j\frac{\partial}{2}} = V\left(\cos\frac{\partial}{2} - j\sin\frac{\partial}{2}\right) \text{ And}$$

$$V_{pq} = Ve^{j\left(\frac{\partial}{2}+\rho\right)} = V\left\{\cos\left(\frac{\partial}{2}+\rho\right) + j\sin\left(\frac{\partial}{2}+\rho\right)\right\}.$$

$$P(\partial,\rho) = P_0(\partial) + P_{pq}(\rho) = \frac{V^2}{x}\sin\partial - \frac{VV_{pq}}{x}\cos\left(\frac{\partial}{2}+\rho\right) \qquad (4)$$

$$Q_r(\partial,\rho) = Q_{0r}(\partial) + Q_{pq}(\rho) = \frac{V^2}{x}(1-\cos\partial) - \frac{VV_{pq}}{x}\sin\left(\frac{\partial}{2}+\rho\right) \qquad (5)$$

Table 1. Load on the buses

Sr. No	Load	Bus	System Voltage	Active load (MW)	Reactive load(MVAR)
1	Load 1	Bus 2	11 KV	21.7	12.7
2	Load 2	Bus 3	11 KV	94.2	19
3	Load 3	Bus 4	11 KV	47.8	0
4	Load 4	Bus 5	11 KV	7.6	1.6
5	Load 5	Bus 6	11 KV	11.200	7.5
6	Load 6	Bus 9	11 KV	29.50	0
7	Load 7	Bus 10	11 KV	9.00	5.80
8	Load 8	Bus 11	11 KV	3.5	1.8
9	Load 9	Bus 12	11 KV	6.1	1.6
10	Load 10	Bus 13	11 KV	13.5	5.8

4. UPFC shunt and series converters control

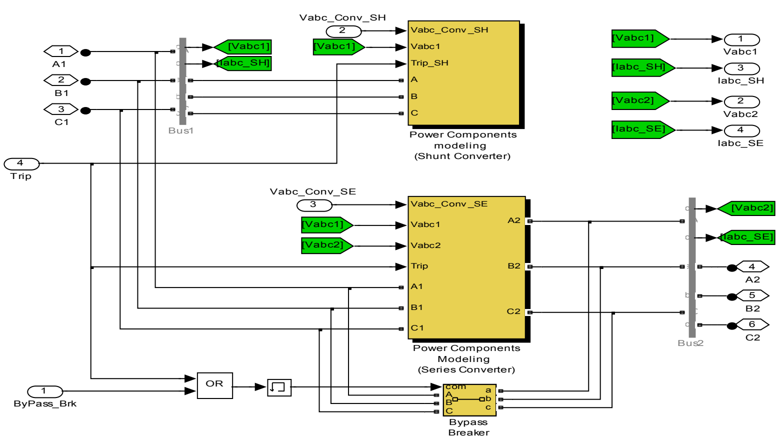

Figure 2. Double loop PI controller for series and shunt converter.

The improved double loop PI Control based approach is used for controlling the series and parallel converter of UPFC.

5. Simulation and Result Analysis

IEEE-14 consists of 14 bus, 5 synchronous machines out of which three are synchronous condenser.259 MW and 81.3 MVAR total active and reactive power demand, respectively & There are 11 loads in the system. Using MATLAB simulink The simulation model of IEEE 14-bus system design using MATLAB/SIMULINK software .The simulation block diagram of the system has been shown in above fig.3 This model has been used to find three phase bus voltages under with and without fault and at different loading with and Without UPQC. Hence, bus-5 was considered as the optimal location for the placement of UPFC Comparative analysis of bus voltage, active and reactive with and without UPFC have been done.

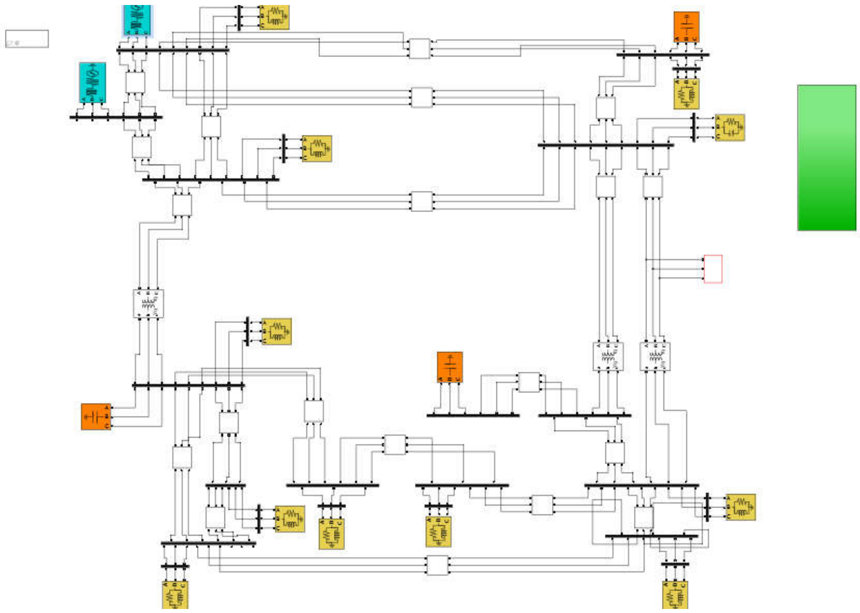

Figure 3. IEEE-14 bus system without UPFC.

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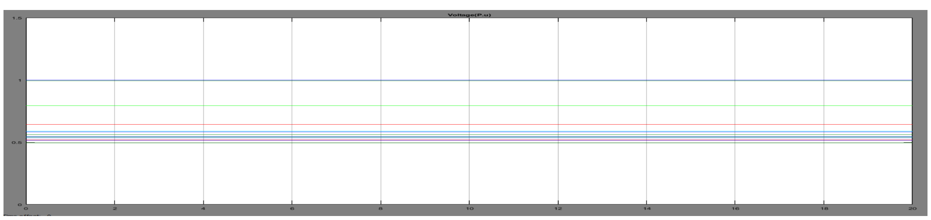

Figure.4 IEEE 14 bus voltage without UPFC

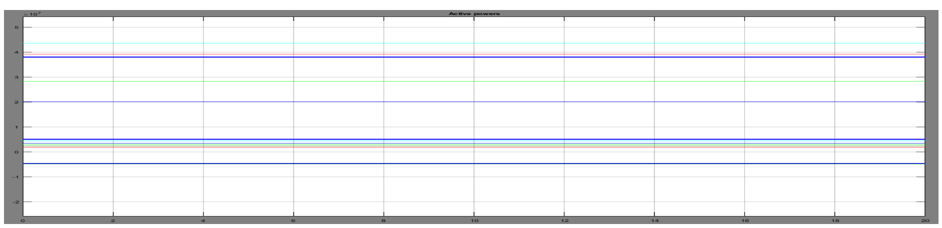

Figure 5. Active power Without UPFC

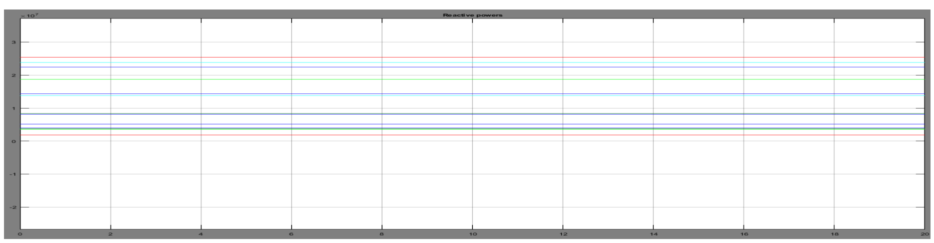

Figure 6. Reactive power without UPFC

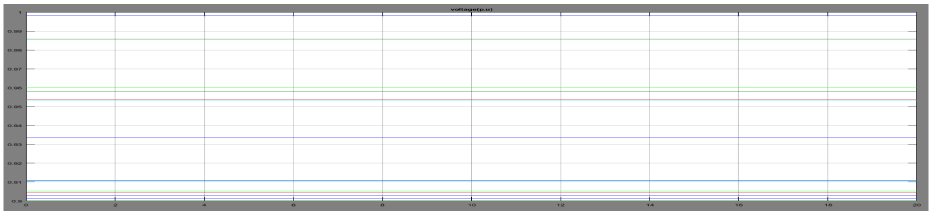

Figure7. voltage with UPFC

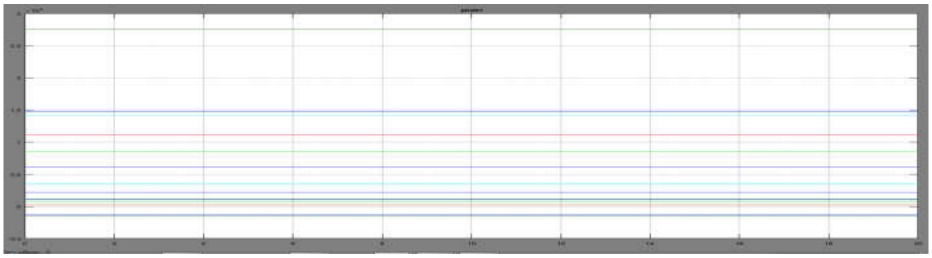

Figure 8. active power with UPFC

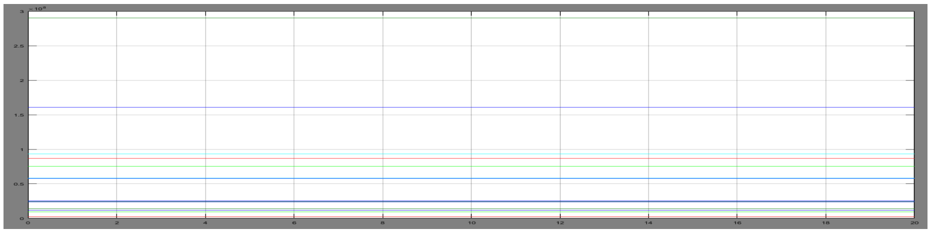

Figure 9. reactive power wth UPFC

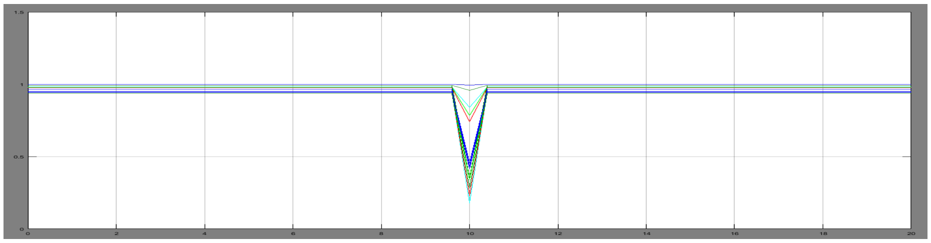

Figure10. Bus voltage at fault condition without UPFC

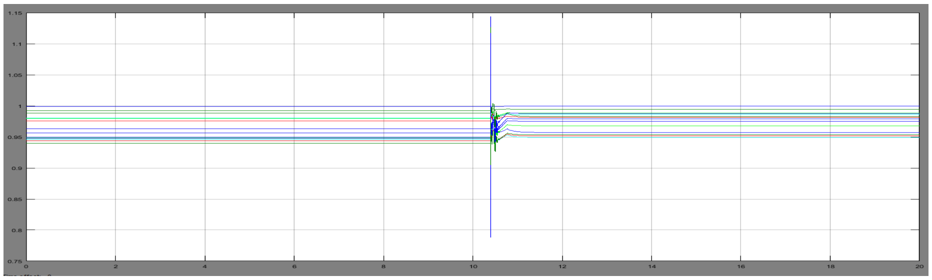

Figure 11. Bus voltage at fault condition with UPFC

Table 4. Comparative of Voltages,Active power, Reactive power with & without UPFC

BUS	Voltage without upfc(p.u)	Active power without upfc(W)	Reactive power without upfc	Voltage with upqc(p.u)	Active power with upfc(W)	Reactive power with upfc
1	0.99	6.45e7	5.98e7	0.999	3.79 e7	2.23e7
2	0.994	1.31e8	1.23e8	0.993	1.79 e8	1.52e8
3	0.985	8.32e7	4.80e7	0.589	4.36 e7	2.38 e7
4	0.981	3.46e7	3.33e7	0.643	3.92 e7	2.54 e7
5	0.98	3.22e7	2.75e7	0.793	2.82 e7	1.86 e7
6	0.987	2.13e7	5.62e7	0.583	2.00 e9	1.43 e7
7	0.957	1.43e7	2.48e7	0.546	4.69e6	8.09 e7
8	0.982	1.47e7	2.55e7	0.581	4.80 e6	8.31 e6
9	0.949	7.45e7	4.80e7	0.536	4.43e6	1.37 e7
10	0.951	-1.67e7	1.043 e7	0.513	1.80 e6	1.796e6
11	0.967	1.34 e7	1.615 e7	0.542	2.97 e6	3.57 e6
12	0.979	5.56e6	1.09 e7	0.535	3.43e6	3.93 e6
13	0.975	8.93e6	2.63 e7	0.516	5.08 e6	5.09 e6
14	0.953	2.366e7	8.36 e6	0.493	2.30 e6	3.72e6

6. Conclusion

This paper presented IEEE-14 with and without UPFC. It is found that double loop pi Control based optimal location of UPFC at bus 4-5 show the power transfer capability of line is more.IEEE-14 bus system with voltages, Active Power and Reactive power for system with UPFC and Without UPFC is validated on MATLAB simulink. System with UPFC show improvement in voltage and power transfer at buses.