

DESIGN AND ANALYSIS OF LOW-VOLTAGE LOW-POWER DOUBLE-TAIL COMPARATOR AND IMPLEMENTATION OF 3BIT FLASH ADC

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Abstract— High speed dynamic comparators are used in low power and area efficient analog to digital converters to improve speed and power efficiency. Speed and power consumption are the two factors that define the comparators accuracy. A comparator is a device which compares two voltages or currents and outputs a digital signal indicating which is larger. In this paper, a new dynamic comparator is proposed by modifying the low voltage low power double tail comparator circuit for power efficient and high speed operation. In the proposed dynamic double tail comparator system both the power dissipation and delay time would be significantly reduced. The simulations are carried out in MENTOR GRAPHICS, Schematic editor, Generic GDK, 130nm technology. From this it is evident that with the proposed comparator design there is 55.5% in delay and 35.5% reduction in power dissipation. A 3bit flash analog to digital converter is implemented by using existing double tail comparator and proposed comparator.

Keywords— double tail comparator, High speed analog to digital converters, Priority Encoder, Resistor ladder.

Introduction

Comparator is one of the fundamental building blocks in most of the analog-to-digital converters (ADCs). Many of the high-speed ADCs, such as flash ADCs, require high-speed, low-power comparators with small chip area. High-speed comparators in ultra deepsub-micrometer (UDSM) CMOS technologies suffer from very low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [2]. Hence, designing of high-speed comparators is more challenging when supply voltage is smaller. In other words, in this technology, to achieve high speed, larger transistors are required to compensate the reduction of the supply voltage, which also means the more die area and power is needed. Besides, low-voltage operation results in the limited common-mode input range, which is important in high-speed ADC architectures, such as flash ADCs.

The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison. V_p is the input voltage (pulse voltage) applied to the positive input terminal of comparator and V_n is the reference voltage (constant DC voltage) applied to the negative terminal of comparator.

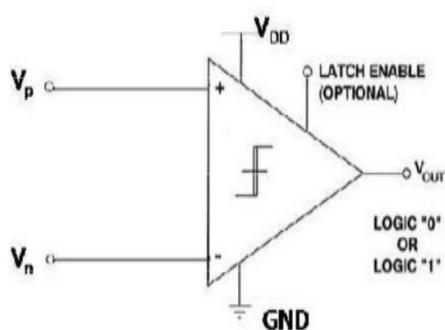


Fig: Schematic of Comparator

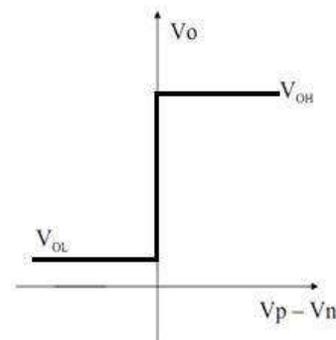


Fig: Ideal voltage transfer characteristic of comparator

BLOCK DIAGRAM OF COMPARATOR

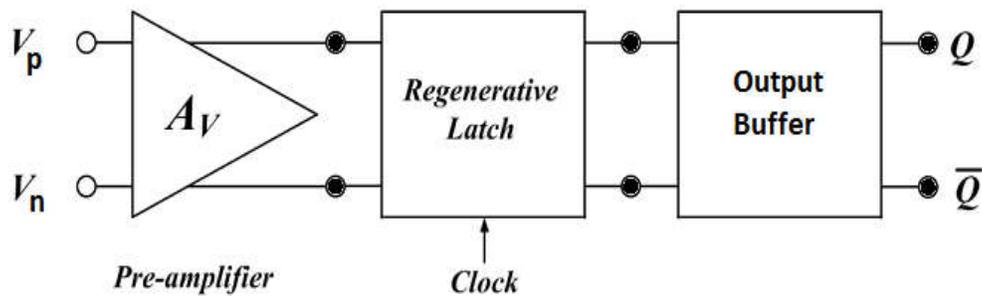


Fig: Block diagram of Comparator

A clocked comparator generally consists of two stages. The first stage is to interface the two input signals. The second stage (regenerative stage) consists of two cross coupled inverters, where each input is connected to the output of the other one. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched by either NMOS or PMOS transistor [3]. If comparator speed is a priority, the regenerative stage could be designed to start its operation from the midway between power supply and ground. For example, in conventional comparator however, the static power consumption reduction, hence transistor count increases there by reducing the speed.

IREVIEW OF EXISTING COMPARATORS

A. Conventional Dynamic Comparator

The schematic circuit of Conventional dynamic comparator is shown in fig.1. The operation of the conventional dynamic comparator is as follows: During pre-charge phase (CLK = 0) and Mtail transistor will be off, the transistors M7 and M8 will pull both the Outn, Outp (output nodes) to VDD in order to define a start condition and to have a valid logical level during reset [1].

During evaluation phase (when CLK = VDD) transistors M7, M8 are off and corresponding Mtail transistor will be on. Output nodes (Outp, Outn) which had been pre-charged to VDD, start to discharge at different discharging rates depending on the input voltages (VINP and VINN). Assuming the case where VINP > VINN, the output node Outp start to discharge at a faster rate than Outn, hence Outp (discharged by transistor M2 drain current), falls down to 'VDD - |Vthp|' before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M5) will turn on to initiate the latch regeneration with the help of two back-to-back inverters (M3-M5 and M4-M6). Thus, the output node Outn will be pulled to VDD and Outp discharges to ground. If the input voltage VINP is less than VINN, the circuit works vice versa [3].

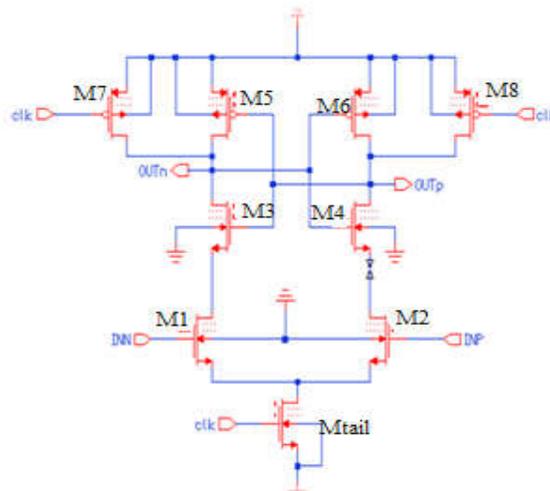


Fig 1: Schematic Circuit of Conventional dynamic comparator

The main advantage of Conventional dynamic comparator is high input impedance, rail-to-rail output swing, and no static power consumption.

II.PROPOSED COMPARATOR

The schematic circuit of proposed comparator is as shown in fig 5. The operation of the circuit is as follows: During pre-charge(reset) phase $clk=0$, both M9 and M10 pmos transistors are turned on and they pull fp and fn node capacitances to VDD, which turns on both M5 and M8 nmos transistors and make fp and fn nodes to discharge to ground. Sequentially pmos transistors M1, M2 turn off and they make outp and outn nodes to be discharged to ground. During evaluation (decision) phase $clk=VDD$, fp and fn node capacitances are discharged from VDD to ground in a different time rate proportion to the magnitude of each input voltage [9]. As a result, an input dependent differential voltage is formed between fp and fn nodes. Once either fp or fn node voltage drops down below a value small enough to turn off M5/M8 the corresponding output nodes will be charged to VDD. If $V_{inp} > V_{inn}$ the outp will be high and it is low otherwise.

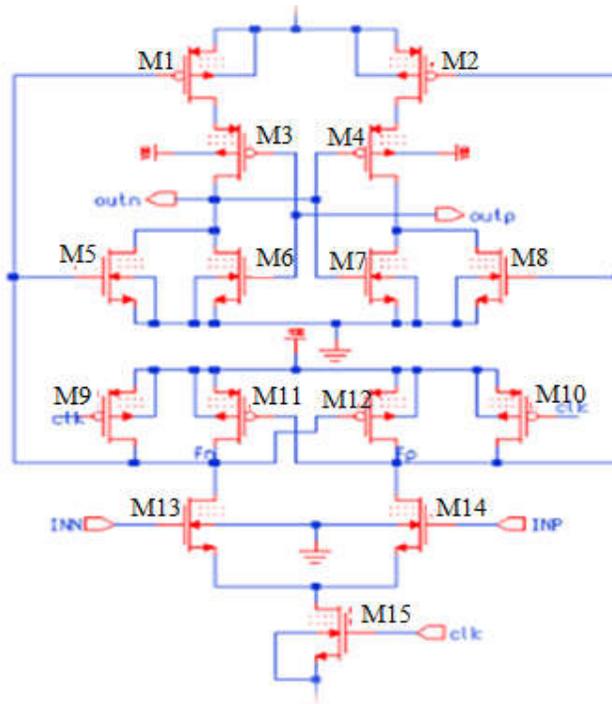


Fig 5: Schematic circuit of proposed comparator

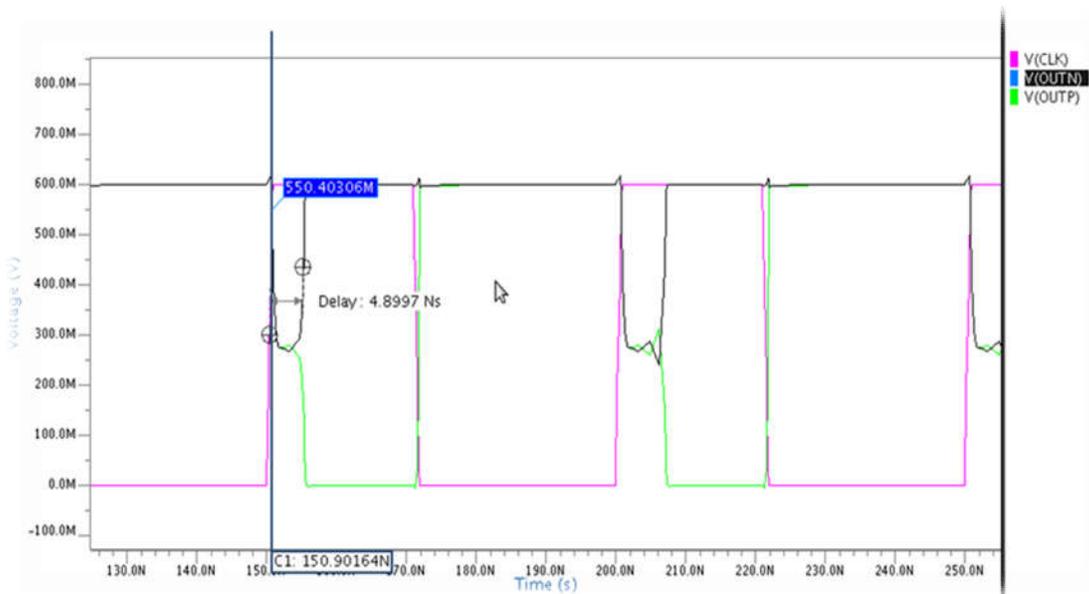


Fig 6: simulation waveform

III.SIMULATION RESULTS AND PERFORMANCE COMPARISONS

All the comparators were designed using Chartered Semiconductor Limited's 0.13 μ m CMOS process technology, at a supply voltage of 0.6V and 0.8V, using MENTOR TOOLS. The performance of the proposed comparator is evaluated and compared with existing comparators. Table I summarize the performance of the reviewed existing comparators and proposed designs.

SNO	Rise Time 0.6v 0.8v	Fall Time 0.6v 0.8v	Delay 0.6v 0.8v	Power dissipation 0.6v 0.8v	No. of transistors used
Conventional dynamic comparator	800.00ps 307.08ps	4.6343ns 424.94ps	4.8997ns 29.541ns	496.967pw 667.354pw	09
Conventional double tail dynamic comparator	800.00ps 800.00ps	800.00ps 800.00ps	216.15ps 242.26ps	1.5669nw 1.0896nw	12
Modified Double Tail Comparator a) Main Idea	800.00ps 800.00ps	800.00ps 800.00ps	1.5949ns 49.768ns	1.0588nw 1.521nw	14
Modified Double Tail Comparator b)Final Structure	800.00ps 800.00ps	99.301ps 99.301ps	185.54ps 20.503ns	1.0590nw 1.514nw	16
Proposed comparator	800.00ps 800.00ps	429.89ps 800.00ps	429.89ps 424.34ps	540.060ps 735.31ps	15

IV. APPLICATIONS

Comparators are the key design elements for a wide range of applications such as

- Analog to digital converters.
- Test circuit applications.
- Schmitt trigger.

Flash A/D Converter:

A flash ADC is a type of analog-to-digital converter shown in below fig.7,which uses a linear voltage ladder and a comparator at each ladder to compare the input voltage with that of successive reference voltages. Often these reference ladders are constructed using many resistors. The output of these comparators are generally fed into a digital encoder, which converts these inputs into a binary value. Flash converters are extremely fast compared to other types of ADCs.

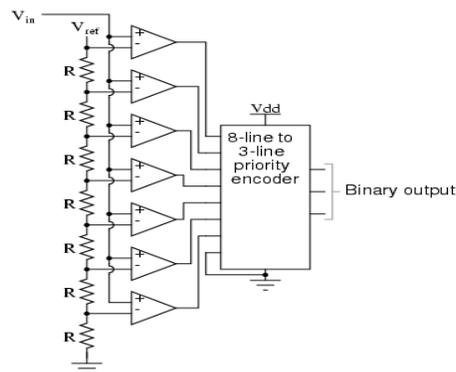
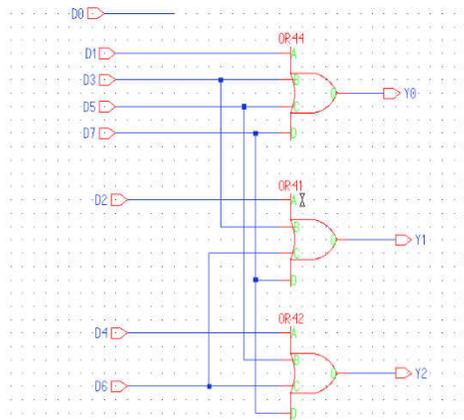


Fig 7: 3-Bit Flash ADC



Priority encoder block

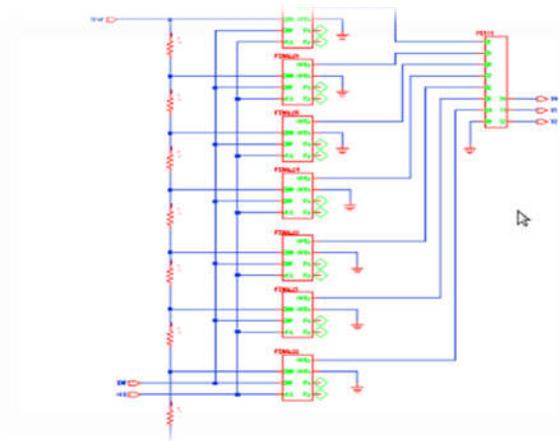


Fig 8: Schematic circuit of 3-bit Flash ADC with existing comparator

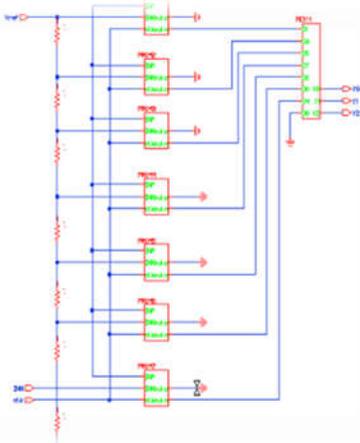


Fig 9: Schematic circuit of 3-bit Flash ADC with proposed comparator

COMPARISON TABLE-II

Parameters	3- Bit Flash ADC	3- Bit Flash ADC
Rise Time	800.00ps	800.00ps
Fall Time	800.00ps	800.00ps
Delay	48.957Ns	27.752Ns
Power Dissipation	3.571Nw	3.254Nw

V.CONCLUSION

In this paper, comprehensive delay analysis for clocked dynamic comparators were presented. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Based on double tail structure a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Pre-layout simulation results in 0.13- μ m CMOS technology confirmed that the delay and power dissipation of the proposed comparator is reduced to a great extent in comparison with the existing comparators. By implementing 3bit flash analog to digital converter using existing double tail comparator and proposed comparator a delay of 56.5% and power dissipation up to 30.5% is reduced.

REFERENCES

- [1] BabayanMashhadi, S. Reza Lotfi “Analysis and Design of a Low-Voltage Low-PowerDouble-Tail Comparator”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems,Vol:22, Issue:2, Page(s):343-352, feb.2014.
- [2] Babayan Mashhadi, S.Lotfi,R. “Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator” IEEE Transactions on Very Large Scale Integration(VLSI) Systems,Vol:22,Issue:2,Page(s):343-352,feb.2014.
- [3] B. Goll and H. Zimmermann, “A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65”, *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.
- [4] Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, “Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators”, *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 56, pp. 911-919, May 2009.
- [5] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Van der Plas, “Noise analysis of regenerative comparators for reconfigurable ADC architectures”, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6,pp. 1441–1454, Jul. 2008.
- [6] Daniel Schinkel, EisseMensink, Eric Klumperink, Ed Van Tuijl, Bram Nauta, “A Double tail latch type voltage sense amplifier with 18ps setup + hold time”, *IEEE*, 2007.
- [7] P. M. Figueiredo and J. C. Vital, “Kickback noise reduction technique for CMOS latched comparators”, *IEEE Trans. Circuits Syst. II, Exp.Briefs*, vol. 53, no. 7, pp. 541–545, Jul. 2006.
- [8]B.Wicht, T.Nirschl, and D. Schmitt-Landsiedel, “Yield and speed optimization of a latch type voltage sense amplifier”, *IEEE J.Solid State Circuits*, vol.39, pp.1148-1158, July2004.
- [9] P.Amaral, J.Goes, N.Paulino, and A.Steiger-Garcia, “An improved low-voltage low power CMOS comparator to be used in high-speed pipeline ADCs”, in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, vol. 5, pp. 141–144.
- [10] Sougata Ghosh, Samraat Sharma, “A Novel Low-Power, Low- Offset and High-Speed CMOS Dynamic Latched Comparator”, *International Journal of Electronics and Computer Science Engineering*, IEEE, 2010, Vol. 2, Number 1, pp. 411-426.