BCD ADDER ENTERPRISE EXHAUSTING NOVEL REVERSIBLE LOGIC FOR STUMPY POWER APPLICATIONS

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ABSTRACT:

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. This paper presents an optimized reversible BCD adder using a new reversible gate. A comparative result is presented which shows that the proposed design is more optimized in terms of number of gates, number of garbage outputs and quantum cost than the existing designs

INTRODUCTION:

Reversible logic is an interesting area, which is highlighted due to its involvement in numerous technological design implementations. It is one of the potential techniques in the field of nano scale engineering where power dissipation reduction is a major criteria. The existing technologies are more prone to the heat dissipation, which is a major disquiet from the point of designer as well as end user. When the designer introduces a new design, as example mobiles, which include highly scalable technology may use impractical and in adequate range of parameters such as voltage or temperature. The major advantage of any design with reversible logic is complete reduction of power dissipation, which results in zero heat-generated products. Investigations based on irreversible logic shows that the energy lost on every bit of information is kTln2 joules; where T is absolute temperature and k is Boltzmann constant.1 Such energy lost would not occur if the process uses reversible method.2 This is because the amount of energy that is dissipated has a direct connection with the number of bits that are erased during the computation. This result in a circuit with reversibility technique, in which any bit of information will not lose energy while employing the reversible computation, where

as the reversible computation is performed using reversible gates.3,4 Despite of their large area, reversible gate designs are proved their low power advantage compared to their counter designs using CMOS logic. The important measuring parameters for logic design using reversible gates includes the number of gates used for the design with less number of unused outputs also called as garbage outputs. The optimized design also concerned about minimum number of inputs, which are left constant. The crucial design aspect for reversible logic lies in reduction of number of unused outputs because the accumulation of garbage by at least single digit causes an exhaustive and excessive execution of the circuit. Hence, a very important design aspect of reversible logic is to use less number of garbage bits. One of the design aspects behind reduction of garbage outputs is to use large number of gates in the circuitdesign. Dynamic programming is the one that allows

the user with lowest garbage count during the synthesis step. Circuit that uses Toffoli and Fredkin reversible gates results in minimal garbage. Switches that use “don’t cares” also results in minimal garbage. Quantum technologies are the one that may use reversible logic. An example of complex antenna simulation design in which reversible logic is implemented in hidden but may not be seen as a separate logic. However, the importance of simulation reveals the reversible transformation in the process of propagating a wave.

MATERIALS AND METHODS

In this paper, BCD adder is implemented in two ways primarily using logic gates in traditional way and the same using reversible logic Gates, the corresponding flowchart shown in Figure 1 represents algorithm steps required.

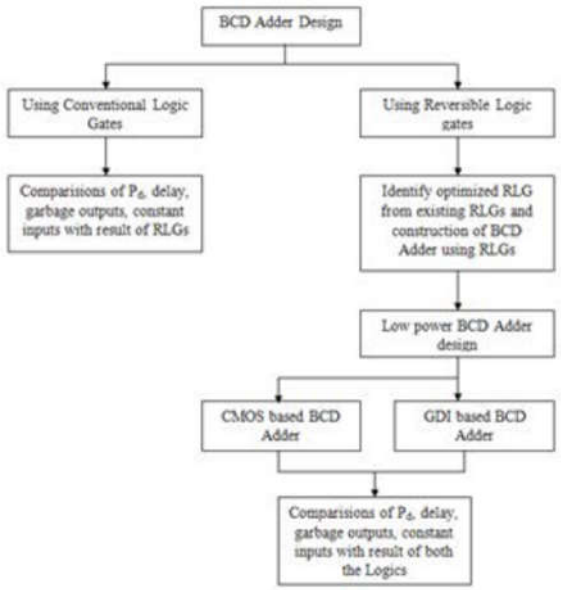


Figure 1. Flowchart.

Traditional BCD Adder

The traditional BCD adder is implemented by considering logic gates as shown in Figure 2. It uses

two 4-bit adders and one correction circuitry in which OR and AND Gates were used.

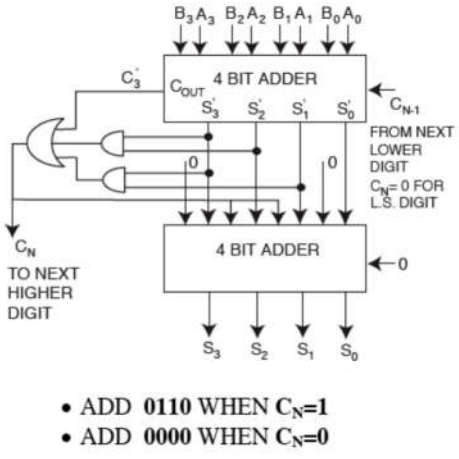


Figure 2. Conventional BCD Adder

DESIGN OF BCD ADDER USING RLG

Reversible Logic Gates (RLG) is differentiated based on their complexity and input/output relation. Basic RLG's exists with sizes from minimum 2x2 to maximum 5x5 input/output combinations. The proposed work considered three types of RLG's namely HNG, TSG and BBCDC for the design of BCD adder.5

HNG GATE

A HNG (Hybrid New Gate) is a basic RLG gate, which uses four variables for input/output combinations as shown in Figure 3. The best implementation of this gate isripple carry adder since using single gate itself it produces sum as well as carry output hence reduces the number of garbage and gate counts

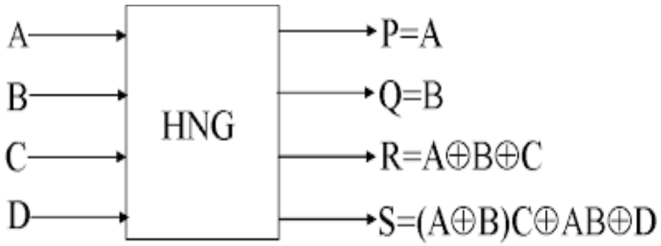


Figure 3. HNG 4x4 Gate.

TSG Gate

Figure 4 shows TSG gate implementation for full adder. If the input C is made zero then the circuit acts like a full adder and the output R gives the sum and the output S gives the carry out.

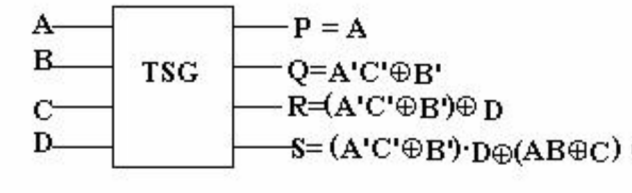


Figure 4. TSG 4x4 Gate.

BBCDC Gate

A BBCDC (Binary to BCD conversion) is a 5X5 reversible gate shown in Figure 5, is used in the implementation of BCD adder.9 Table 1 shows the corresponding input/ output vectors. Design of BCD adder using reversible BBCDC gates is shown in Figure 6, which requires a minimum of nine inputs A0-3, B0-3 and five outputs in which four bits are for sum bits S0, S1, S2, S3, and Cout.5-17 Four bits are required to code the augends, which makes eight bits, and including circuit carry bit it makes the nine bits input.

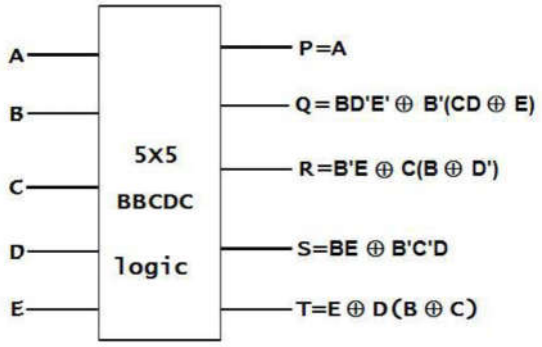


Figure 5. BBCDC 5x5 Gate.

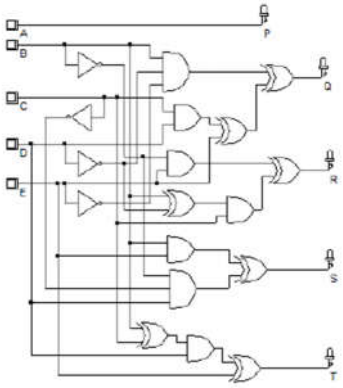


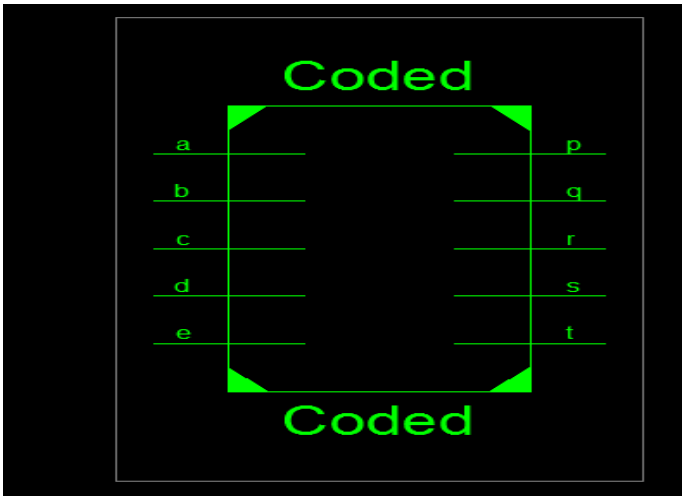
Figure 6. BBCDC 5x5 Gate.

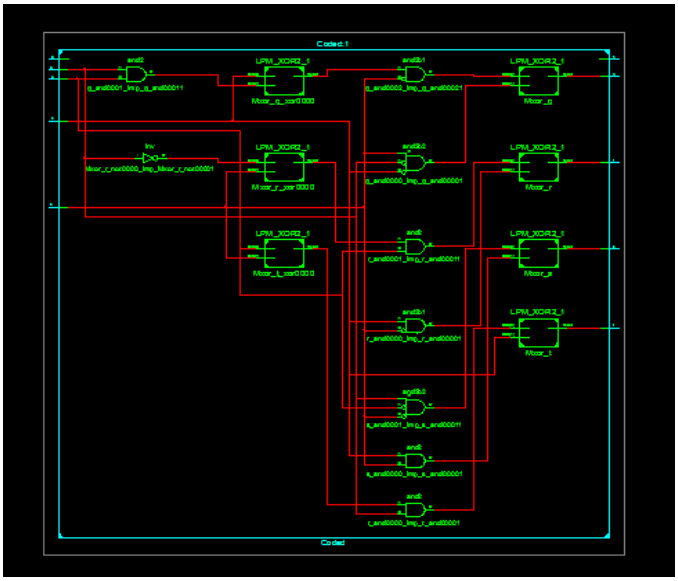
Table 1. Truth table of BBCDC Gate

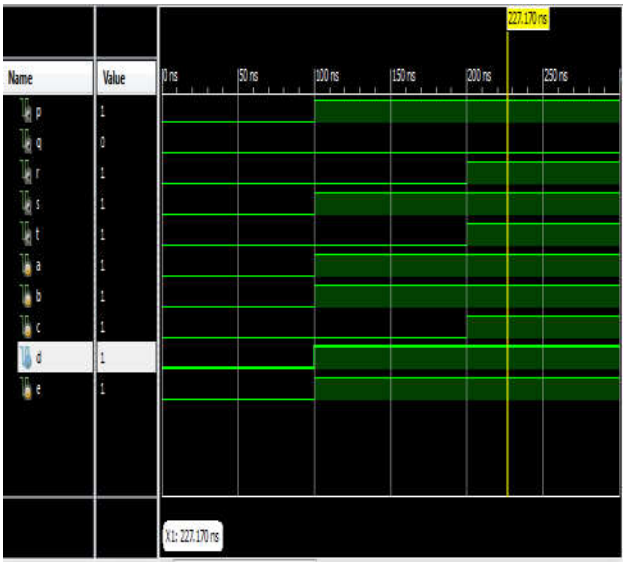
Inputs					Outputs				
E	D	C	B	A	T	S	R	Q	P
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

Consider adding 9+9+1 in decimal, gives 19, instraight binary this should produce an output of 100112,but this is an invalid number in BCD. Because in BCDcode the four bits binary which only represents decimal numbers 0-9. Table1 shows decimal numbers 0-19 with their binary and BCD codes.

SIMULATION RESULTS:







CONCLUSION

Low power BCD adder was implemented using BBCDC reversible logic. Different parameters such as number of unused outputs, constant inputs, delay, area, number gates used, power, and PDP are compared for different BCD adder logic designs

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