A HIGH-SPEED AND POWER EFFICIENT VOLTAGE LEVEL SHIFTER FOR DUAL SUPPLY APPLICATIONS

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ABSTRACT: This short provides a rapid as well as power-efficient voltage levelshifting circuit efficient in transforming incredibly reduced degrees of input voltages into high outcome voltage degrees. The efficiency of the proposed circuit is because of the truth that not only the stamina of the pull-up device is considerably minimized when the pull-down tool is taking down the outcome node, yet the stamina of the pull-down device is likewise increased utilizing a low-power auxiliary circuit. Postlayout simulation results of the proposed circuit in a 0.18- μm modern technology show an overall power per transition of 157 fJ, a static power dissipation of 0.3 nW, as well as a proliferation hold-up of 30 ns for input frequency of 1 MHz, reduced supply voltage degree of VDDL = 0.4 V, and also high supply voltage level of VDDH = 1.8 V.

Key Terms: Level converter, low power, subthreshold operation, voltage level shifter.

1. INTRODUCTION

Power effectiveness and also rate are major factor of efficiency in all digital circuits. Numerous strategies have actually utilized to lower vibrant and also static power. On the other hand, minimizing the supply voltage enhances the propagation delay of the circuits [2] In order to avoid these problems dual supply style are introduced in which a reduced voltage is supplied for the blocks on the noncritical paths while a high supply voltage is applied to the analog and also the highspeed digital blocks. Several of one of the most commonly made use of strategies is vibrant voltage scaling running to near threshold voltage degrees and supporting multiple voltage domains. That is why Level moving circuit is required to supply specific voltage degree for the circuit. A voltage degree shifter is one of the major

components in a digital system. Degree shifters are made use of for provide proper voltage degree for each part in the electronic circuits. A variety of degree shifters have been suggested in the literary works review. Designers move their focus to execute a voltage level shifter, which operates minimum power intake and also maximum rate. Additionally the degree shifter must able to run appropriately for subthreshold input signals. Some of the recently reported high efficiency voltage level shifters are reviewed. The recommended circuit introduced in section 3. Section 4 presents the simulation result of the changed circuit validating the effectiveness of the proposed circuit. Ultimately, ended in area 5. Circuit designers are faced with the obstacle of creating systems with raising performance and also intricacy while under demanding power as well as time-to-market restraints. Such systems commonly need voltage degree translation devices to allow interfacing between integrated circuit tools constructed from different process modern technologies. The option of the correct voltage degree translation device relies on lots of aspects and also will certainly influence the efficiency and also performance of the circuit application. Thus voltage level shifters play an essential role in widely used VLSI systems. Voltage degree translation is required when two tools have varying supply voltage nodes. 2 possible problems exist. A higher-voltage device may be required to drive a low voltage tool. A lower-voltage gadget may be required to drive a high-voltage gadget. If the reduced voltage gadget is the driver, the circuit normally cannot function effectively without using a translation device.

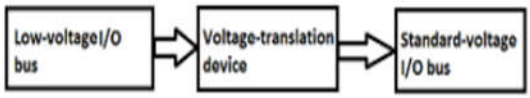

Fig 1: Voltage levelshifter functioning

II. EXISTING LEVEL SHIFTER IMPLEMENTATION

In this area, circuit configuration and also benefits of 2 degree converters lately reported will be quickly described. The procedure of the circuit shown in Fig. 2, is as complies with. When the input signal becomes high transistor Mn1turns on as well as nmos transistor Mn4 switches on due to the fact that the overdrive voltage of Mp3 bigger than the Mn3. Consequently shift current flows Mp1, Mn1, as well as Mn4 and also this present is mirrored to Mp2 and also attempts to bring up the outcome node. Ultimately the output is brought up and the transistor Mp3 switched off consequently nmos transistor

Mn4 take down by the nmos transistor Mn3, suggests no fixed current circulations with Mp1, Mn1, as well as Mn4. If the input is reduced and also INB is high, the nmos transistor Mn2 performs and pulls down the outcome node at the same time nmos transistor Mn1 off and no static current circulations. This indicates that current of Mp2 is not completely close to no weak opinion exist. More lower the value of existing one more gadget Mp4 is made use of.

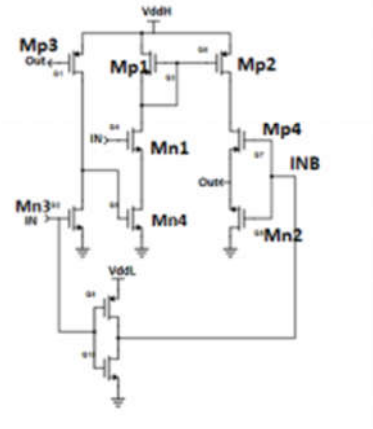

Fig 2: Circuit diagram of voltage level shifter

EXTENSION OF LEVEL SHIFTER WITH AUXILIARY CIRCUIT: In order to further decrease of power and hold-up as an expansion of voltage level shifter with complementary circuit is used, shown in Fig. 2. Complementary circuit transforms just high to reduced transition of input signal and to pull up the node Qc to a worth larger than VddL. Transistor Mn6, Mn7 as well as Mp6 are activated and nmos transistor Mn5 turned off, therefore shift present flows through Mn6, Mn7, Mp6 are mirrors to Mp7 and pull up the node QC.

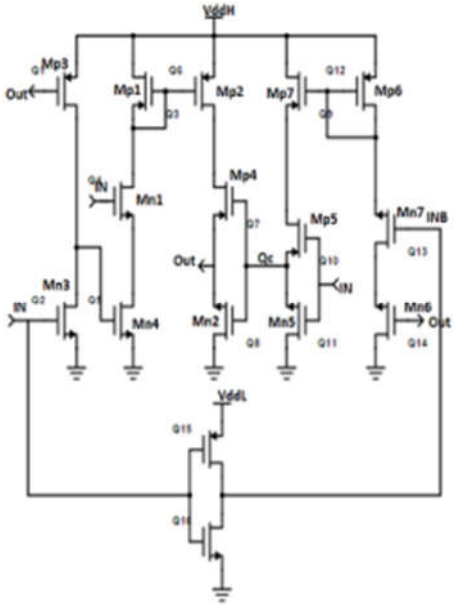

Fig 3: Extension of voltage level shifter with auxiliary circuit

The strength of pull-up tools is substantially reduced when the take down tool is taking down the outcome node, however the stamina of take down tool is additionally increased utilizing a reduced power accessory circuit.

III. PROPOSED MODEL

A new power optimized suggested voltage degree shifter is presented. Here the power gating innovation is applied for power optimization. Power gating is the circuit layout method that has actually been most

commonly made use of in commercial products, indicates connecting sleep transistor to combination of pull up pull down network to minimize the below threshold leakage existing. A rest transistor is dividing the bring up network from Vdd and also pull down network from Vss.

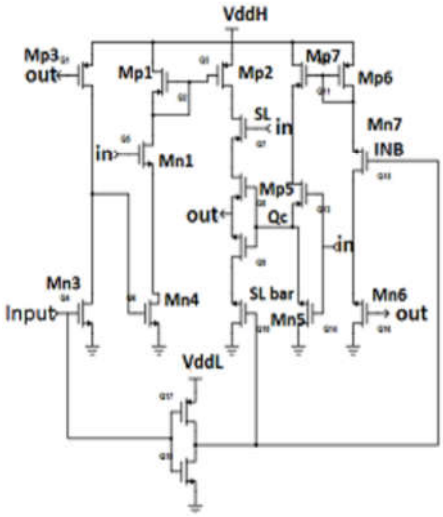

Fig 4: Proposed Voltage level shifter

Rest transistor SL separates transistor Mp4 from Vdd and also SL bar separates nmos transistor Mn5 from Vss. Throughout active setting SL=0, sleep transistor activates as well as offer low resistance in the conduction path. Circuit cut off from its power supply in sleep setting SL=1 by means of existing switch. In order to better decrease the worth of IP2, one more device, i.e., MP4 in Fig. 2(a) is utilized. For more information, when MN2 is taking down the result node, the gate of MP4 is "High" with the worth of VDDL and consequently the drainpipe-- resource voltage of MP2 is decreased. Because of this, as shown in Fig. 3, the propagation delay as well as for that reason the power dissipation of the circuit will be lowered. It must be noted that if evictions of MN2 and also MP4 are driven with a voltage higher than VDDL, not only the current of the pull-up tool (i.e., IP2) is considerably reduced, but likewise the stamina of the pull-down device (i.e., MN2) is increased. Thus, the contention and as a result the delay and the power (particularly the power consumption of the next stage) are considerably decreased. Furthermore, the degree shifter will certainly have the ability to run correctly also for subthreshold input voltages. In order to apply this technique to the recommended framework, as received a complementary circuit (i.e., MP5, MP6, MP7, MN5, MN6, as well as MN7) is made use of. This supporting circuit turns on only in the high-to-low change of the input signal to pull up the node QC to a value larger than VDDL. The procedure of this component of the circuit is as complies with. When IN modifications from "High" to "Reduced" and also OUT is not still representing the input logic level, MN6, MN7, and MP6 are switched on and also MN5 is switched off. Therefore, a transition existing circulations through MN6, MN7, MP6, and also mirrors to MP7 (i.e., IP7) pulling

up the node QC. This suggests that MP4 is turned off and also MN2 is activated with a voltage greater than VDDL, as received bring about a substantial reduction in the aforementioned contention. Finally, when OUT is taken down, MN6 is switched off as well as subsequently no present circulations with MN6, MN7, and also MP6 definition that the supporting circuit is switched on just throughout the high-to-low shift of the input signal, as displayed in. It must be kept in mind that since it is not required to bill QC up to the specific value of VDDH, the auxiliary circuit is created such that the current moving via MP7 (i.e., IP7) is extremely small. This suggests that the existing opinion in this branch will certainly be minimal, decreasing the proliferation delay and also the power consumption of the supporting circuit. Therefore, making use of the complementary circuit, as received the power usage of the main circuit including the output load circuit (an inverter is added as a tons circuit to all the frameworks) is substantially lowered such that the whole power intake of the proposed framework is just around 30% of that of the framework without the complementary circuit. It can be concluded that the effectiveness of the recommended circuit results from the reality that not only the stamina of the pull-up tool is dramatically decreased when the pull-down tool is taking down the output node, but the toughness of the pull-down gadget is also increased making use of a low-power supporting circuit.

IV. SIMULATION RESULTS

In order to confirm the efficiency of the recommended voltage level shifter, the proposed framework as well as additionally a few other state-of-the-art jobs has actually been substitute in a basic TSMC 0.18-μm 1P6M CMOS innovation.

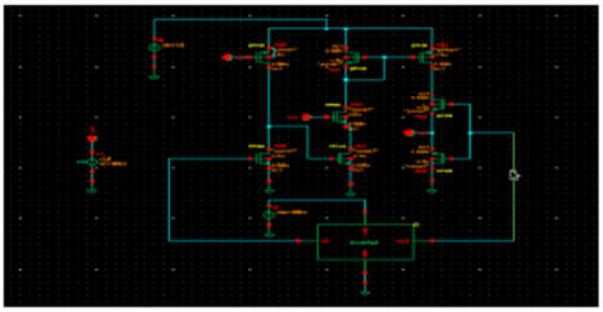

Fig 5: Implementation of voltage level shifter

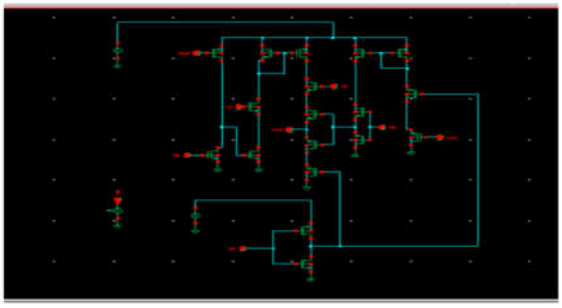

Fig 6: Implementation of Proposed Voltage Level Shifter

Targeting the minimum powerdelay-product (PDP), all the circuits have been efficiently designed to be useful in all

procedure, voltage, and temperature (PVT) edges for VDDL = 0.4 V, VDDH = 1.8 V, and the input frequency of fin = 1 MHz. In the proposed circuit, the shift current of IP2 (in Fig. 2) should be big sufficient to decrease the propagation hold-up of the low-to-high shift of the result voltage. On the various other hands, the power intake of the branch of MP1, MN1, and MN4 must be minimized. Therefore, the existing mirror proportion (i.e., (W/L)P2/(W/L)P1) must be huge. For this function, the length of MP1 has been picked to be 5 μm, whereas the sizes of the other tools are all picked of minimal dimension (i.e., 0.18 μm). Furthermore, the size of MP2 is likewise picked to be 1 μm. Additionally, given that MN2 is driven by a voltage lower than VDDH, it needs to be rather solid to be able to pull the outcome node down. Thus, the width of this transistor is chosen to be 1 μm, while the widths of the various other transistors are of minimum size (i.e., 0.4 μm). It is worth noting that not just the complementary circuit in Fig. 2, however likewise all the other frameworks, particularly the one reproduced from [5] as well as displayed in Fig. 4(a), are likewise created making use of the same strategy. In order to have a reasonable comparison in between the structures, a device buffer and an inverter are added as the tons circuit and input barrier, respectively, to all the structures and the calculated power dissipation consists of the power intake of these barriers. The transistors' dimensions utilized for the efficiency contrast are received Fig. 4. The transistor' sizes of the proposed circuit are shown in Fig. 2. Furthermore, Fig. 5 reveals the format of all the frameworks. The list below outcomes is related to the postlayout simulations.

Frequency	$V_{DDL,min}$ (V)	Power (μW)	Delay (ns)
5 MHz	0.38	0.98	45
10 MHz	0.41	1.68	24.3
20 MHz	0.44	2.77	13.65
50 MHz	0.49	5.72	5.81
100 MHz	0.54	10.2	2.86
200 MHz	0.6	17.66	1.46
500 MHz	0.72	47	0.63
1 GHz	0.9	95	0.34

Table 1: Simulation Results Of the Proposed Circuit (Vddh = 1.8 V)

In the proposed framework, the typical PVT corner entails typicalnMOS and also pMOS transistors, a high supply voltage of VDDH = 1.8 V, and a temperature level of 25 ° C. In addition, slow-nMOS, fastpMOS, VDDH = 1.8% + 10% = 1.98 V, and also a temperature of 0 ° C were chosen as the worst edge. This is because of the fact that a bigger difference between VDDL as well as VDDH along with fast-pMOS as well as slow-nMOS increases the pointed out contention in between the pull-up and also the pull-down tools. Furthermore, in the subthreshold area, a lower temperature level cause a smaller

exists for the gadgets bring about increase the proliferation hold-up. On the other hand, for the very best edge, simulations show that the minimal delay occurred for fastnMOS, fast-pMOS, VDDH = 1.8%-- 10% = 1.62 V, as well as a temperature level of 120 ° C. Fig. 6 reveals the simulation results of the hold-up and the power dissipation of the suggested level shifter versus the value of VDDL, for the common, worst, and best PVT edges. It can be observed that the circuit works correctly in any way the PVT edges for an input frequency of 1 MHz.

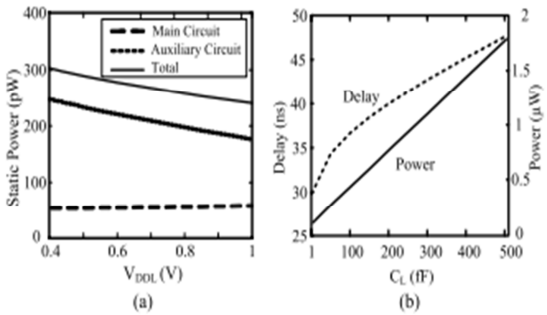

Fig 7: (a) Simulated values of the static power dissipation of the proposed level shifter as a function of VDDL when VDDH = 1.8 V. (b) Total power dissipation and delay of the proposed structure versus the size of the capacitive load (VDDL = 0.4 V, VDDH = 1.8 V, and fin = 1 MHz).

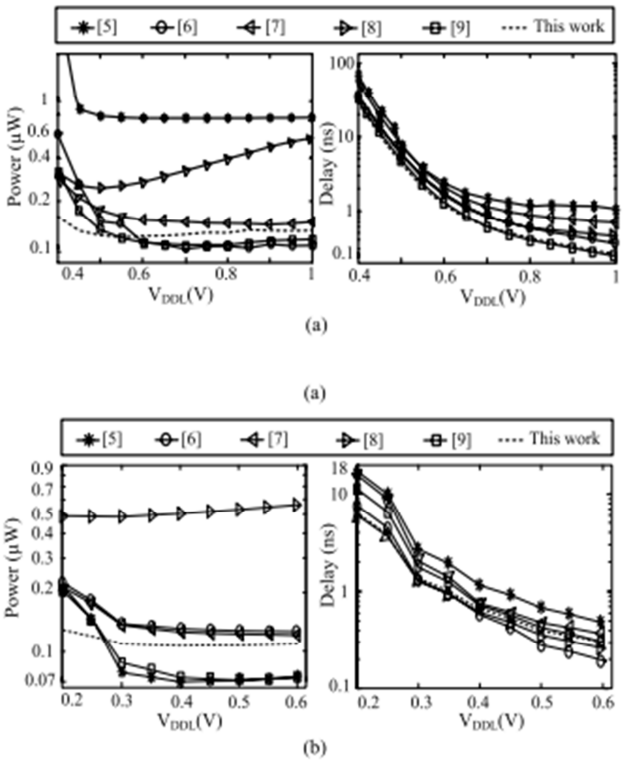

Fig 8: Simulated values of the total power dissipation and delay of the level-shifter structures as a function of VDDL in (a) 0.18-μm CMOS with VDDH = 1.8 V and (b) 90-nm CMOS with VDDH = 1.2 V. The input frequency is 1 MHz. MP7, MP5, and also MN5. It ought to be kept in mind that as VDDL (the driven voltage of evictions of MP5 and MN5) enhances, the drain-- resource voltage of MP7 is lowered causing a smaller sized current in MP7 and consequently a smaller sized static current. Fig. 7(a) contrasts the fixed power eaten by the auxiliary circuit with the main part of the circuit. It can be observed that the huge part of the total static power is eaten by the supporting circuit. Moreover, Fig.

7(b) reveals the power usage and the breeding hold-up of the suggested circuit as a feature of the size of the capacitive tons (i.e., CL). As anticipated, the power as well as the hold-up is boosted linearly with the size of the capacitive tons. the circuit is lowered. The minimum values of VDDL for which the circuit operates appropriately at 100 MHz and 1 GHz are 0.54 V and also 0.9 V, respectively.

V. CONCLUSION

In this brief, a fast as well as low-power voltage level-shifting design was recommended which has the ability to convert extremely low-input voltages. The performance of the recommended circuit results from the reality that not just the current of the pull-up tool is significantly decreased when the pull-down device is pulling down the outcome node, however the toughness of the pull-down device is likewise increased. Postlayout simulation results confirmed the performance of the proposed circuit compared to other works, especially from the power intake viewpoint.

VI. REFERENCES

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