Simulation of 10-T Full Adder based on Degenerate PTL Technology

[1]B.Prathap Reddy, [2]M.Mohan Reddy, [3]K.Sampath Kumar

[1]Asst. Professor, [2]Asst. Professor, [3]Asst. Professor

[1]Dept. of ECE, [1]SREC, Nandyal, India

[1]prathap.bogala@gmail.com [2]mmr.srec@gmail.com [3]ksampath457@gmail.com

Abstract- **In this paper, it is to propose 10 Transistor Full Adder based on degenerate pass transistor logic (PTL). Threshold loss problems are the main drawback in most pass transistor logic family. This threshold loss problem can be minimized by using the complementary control signals. These complementary control signals are obtained by 5-Transistor XOR-XNOR module. By using these complementary outputs we designed parallel prefix adders based on 10-Transistor full adder. Parallel prefix adders are used to speed up the binary addition and these adders are more flexible to perform addition of higher order bits in complex circuits. The transistor level implementation of parallel prefix adders based on degenerate PTL gives better performance compared to CPL and DPL pass transistor logic.**

Index Terms - Power Dissipation, degenerate, complexity, Threshold loss

I. INTRODUCTION

Low power very large scale integration (VLSI) circuits are important for designing of high performance and portable devices. The high speed, small area and low cost are the main considerations of VLSI circuits. The importance of low power is increasing day by day because of changing trend, packaging and cooling cost, portable systems and reliability. In nanometer technology power has become the most important issue because of increasing transistor count, higher speed of operation and greater device leakage currents. Packaging and cooling cost is dependent on the power dissipation of the chip. Now a days there is a more demand on hand held or battery devices like cell phones, laptops and palmtops etc.,. As these devices are battery operated, battery life is primary concern. The reliability is mainly depends on the failure rates of the chip. These failure rates are due to changes in the temperature. Every 10oc raise in temperature roughly double the failure rates. Reliability point of view low power design methodology is extremely important. The arithmetic circuits [2] are designed at transistor level based on different logic design styles. Those are conventional CMOS [3] logic; pass transistor logic, adiabatic logic and gate diffusion input. The details of pass transistor logic families are discussed in section II, and implementation of prefix adders are described in section III. The performance and results are discussed in section IV.

II. PASS TRANSISTOR LOGIC

Basically transistor is used as a switch. To realize the Boolean functions by using transistor as a switch is typically known as pass transistor logic. The advantages of pass transistor [10] based realization are ratio less, lower area due to smaller number of transistors and lesser power dissipation because of no static power and short circuit

power dissipation. Some of the disadvantages of pass transistor logic are higher delay and multi threshold voltage drop. Pass transistor logic family [11] is used to overcome the limitations of pass transistor circuits. Some of the techniques are

1. Insertion of buffers to avoid long delay of a chain of pass transistor logic.

2. Use of swing restoration circuit to overcome multi-threshold voltage drop (vout=vdd-vtn).

3. Use of dual rail logic to generate complementary control signals.

Complementary Pass Transistor Logic (CPL)

The complementary means it has both outputs i .e. f and $\bar{f}$. In this logic two networks are used to realize both f and $\bar{f}$. At the output side we use two inverting buffers and two weak pMOS transistors. These inverting buffers are used to perform restoration logic levels at the output. The pMOS latches are used to perform swing restoration. The basic AND/NAND, OR/NOR and XOR/XNOR [8] gates implemented in CPL are shown in Figure 1.

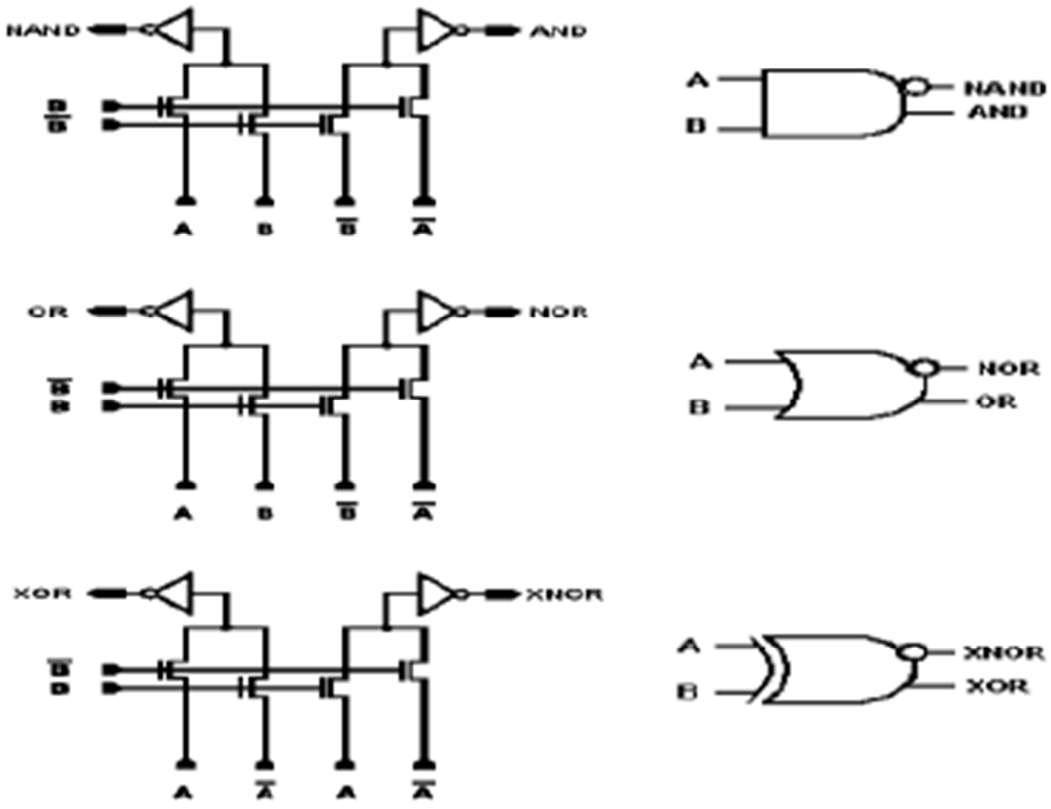

Figure 1. The basic AND/NAND, OR/NOR and XOR/XNOR gates implemented in CPL

Double Pass Transistor Logic (DPL) In double pass transistor [12] logic we are using both nMOS and pMOS transistors are used to design a circuit. Adding of pMOS transistor in parallel with nMOS will produce full swing at the output. The DPL configuration is different from static CMOS logic. The DPL is the modified version of CPL. In this

logic extra transistor is not required for swing restoration. The basic AND/NAND, OR/NOR and XOR/XNOR [9] gates implemented in DPL are shown in Figure 2.

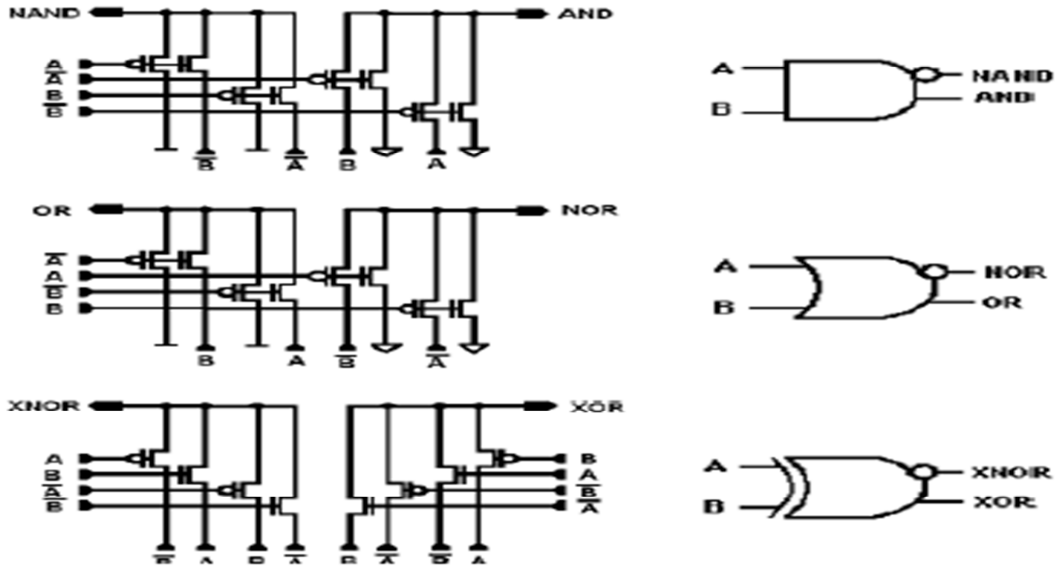

Figure 2. The basic AND/NAND, OR/NOR and XOR/XNOR gates implemented in DPL

Degenerate Pass Transistor Logic Most of full adder [4] designs are based on three module implementation i.e. XOR, sum, carry modules. The 4- Transistor XOR (XNOR) module [5] is used to design a pass transistor logic based full adder [13]. But this type of design raises severe threshold voltage loss problems. The signal degradation in the output causes signal degradation in the further modules. Finally the signal degradation in the circuit causes a multi-threshold loss problem at the output stage. These multi-threshold loss problems can be reduced by using complementary outputs. The complementary outputs are obtained by using 5-Transistor XOR-XNOR design. The design of degenerate 5-T XOR-XNOR module is shown in Figure 3.

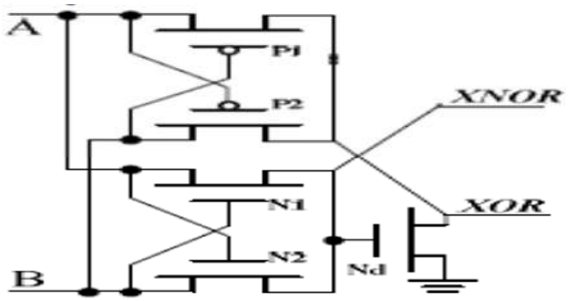

Figure 3. XOR-XNOR designs using 5 transistors

III. PROPOSED ADDER

Pre-possessing stage In this stage we compute, generate and propagate signals to each pair of inputs A and B. These signals are given by the logic equations 1&2:

Pi=Ai xor Bi..... (1)

Gi=Ai and Bi..... (2)

Carry generation network In this stage we compute carries corresponding to each bit. Execution of these operations is carried out in parallel [4]. After the computation of carries in parallel they are segmented into smaller pieces. It uses carry propagate and generate as intermediate signals which are given by the logic equations 3&4:

CPi:j=Pi:k+1 and Pk:j.....(3)

CGi:j=Gi:k+1 or (Pi:k+1 and Gk:j).....(4)

Post processing This is the final step to compute the summation of input bits. It is common for all adders and the sum bits are computed by logic equation 5&6:

Ci-1=(Pi and Cin) or Gi..... (5)

Si=Pi xor Ci-1..... (6)

With the availability of complementary control signals the selection of sum and carry modules [1] are more flexible to avoid the multi-threshold loss problems, the signal degradation in the full adder output is minimized and it is suitable for low vdd applications. The design of degenerate 10-T PTL full adder design is shown in Figure 4.

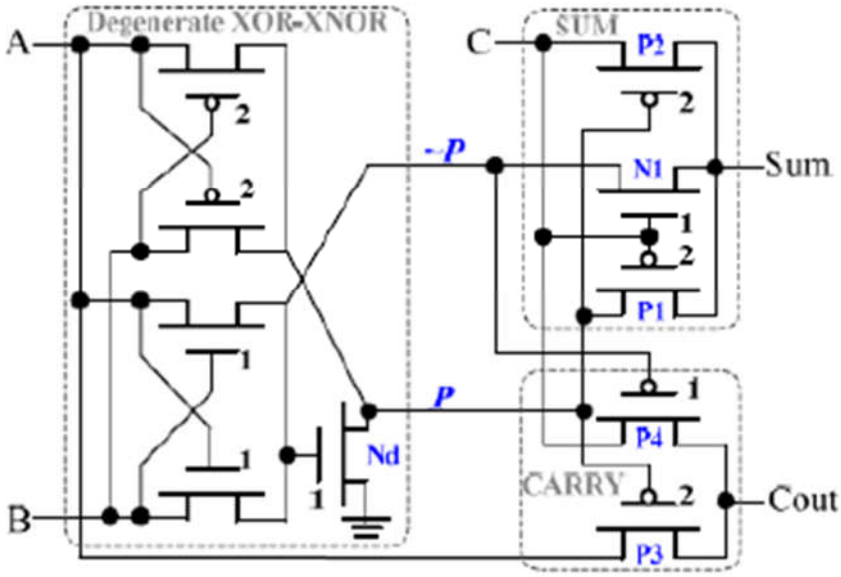

Figure 4. 10-T full adder design using degenerate PTL

The proposed adder is a parallel prefix form carry look-ahead adder. A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is o(log n). It is a fastest adder design and common design for high performance adders in industry.

Transistor level implementation of SUM block and carry operator are shown in Figure 5 and 6

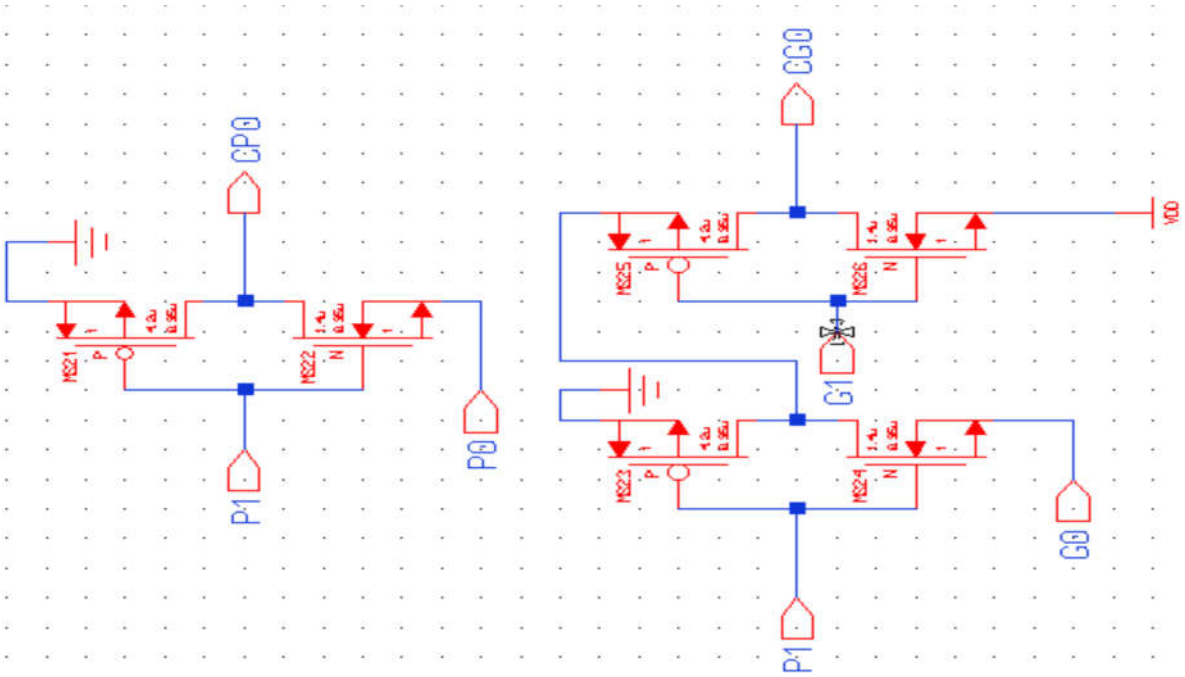

Figure 5.Transistor level implementation of carry operator

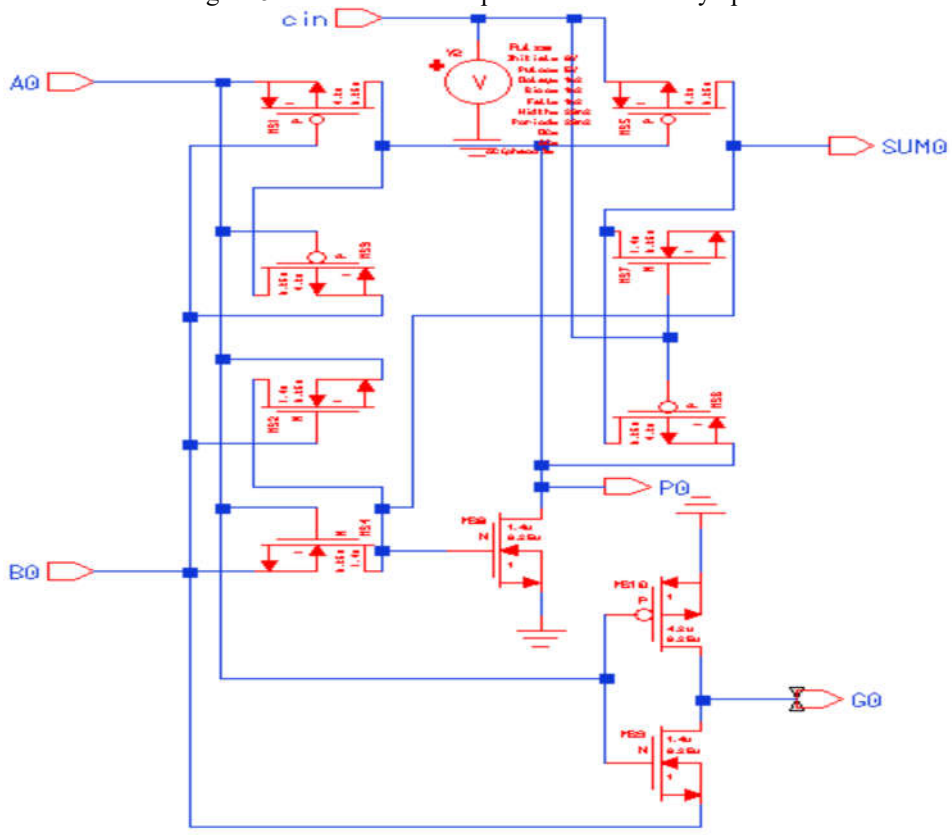

Figure 6.Transistor level implementation of SUM block

IV. SIMULATION RESULTS AND COMPARISONS

The various adders are simulated using SPICE code in Mentor Graphics tool. Adders are designed by using Design Architect in Mentor Graphics tool. The performance of proposed prefix adders in degenerate pass transistor logic are analyzed and compared. The prefix adder architecture is based on the implementation of propagate, generate and carry operator. Simulation results of 10-T adder are compared in terms of DC power dissipation, memory size, number of components and number of steps computed.

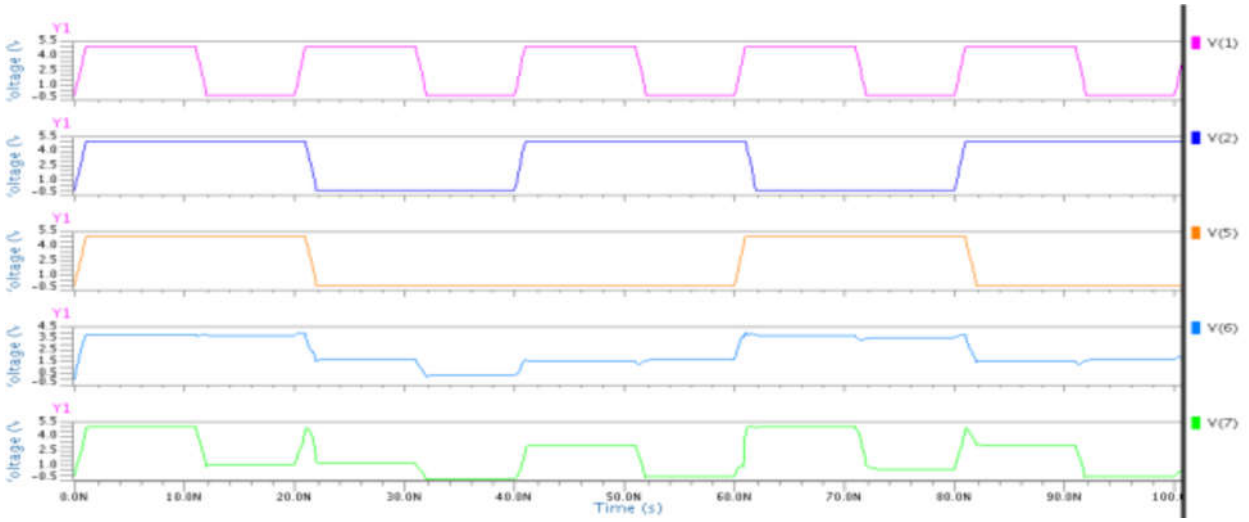

Figure 7. Simulated wave forms of degenerate full adder

V. CONCLUSION

New approach of Degenerate pass transistor logic is used in the design of prefix adders to reduce the Threshold loss problem, power dissipation and signal degradation at the output. The transistor level implementation of prefix adders is simple, lesser power dissipation and high speed compared to other pass transistor logics. The tradeoffs of prefix adders are in terms of power dissipation and area. The simulated result shows that the proposed prefix adder greatly reduces in power dissipation as well as area.

Table 1. Simulation results of degenerate full adder

Parameter	Degenerate Full Adder
Dc power dissipation(mw)	0.05
Memory size(bytes)	43294720
No. of components	13
No. of steps computed	334

REFERENCES

[1] Jin-Fa Lin, Yin-Tsung Hwang and Ming-Hwa Sheu, ―Low Power 10- Transistor Full Adder Design Based on Degenerate Pass Transistor Logic,‖ IEEE Trans. VLSI, vol. 13, no. 6, pp. 686–695, Jun. 2012.

[2] J.-F. Lin, Y.-T. Hwang, M.-H. Sheu and C.-C. Ho, ―A novel high speed and energy efficient 10-transistor full adder design,‖ IEEE Trans. Circuits Syst. I, vol. 54, no. 5, pp. 1050–1059, May 2007.

[3] C.-H. Chang, J. Gu, and M. Zhang, ―A review of 0.18-um full adder performances for tree structured arithmetic circuits,‖ IEEE Trans. VLSI, vol. 13, no. 6, pp. 686–695, Jun. 2005.

[4] Y. Choi, ―Parallel Prefix Adder Design,‖ *Proc. 17th IEEE Symposium on Computer Arithmetic*, pp 90-98, 27th June 2005

[5] H. T. Bui, Y. Wang, and Y. Jiang, ―Design and analysis of low-power 10-transistor full adders using XOR–XNOR gates,‖ IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. vol.49, no. 1, pp. 25– 30, Jan. 2002.

[6] D. Radhakrishnan, ―Low-voltage low-power CMOS full adder,‖ IEE Proc. Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb.2001.