Designing of Binary to Grey Converter QCA Using Nanotechnology

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Abstract- Quantum dot cellular automata (QCA) are leading nanotechnology which has been jumble-salebroadly in digital circuits and systems. It is anencouragingalternate to complementary metal–oxide–semiconductor (CMOS) technology with severalappealingtopographies such as high-speed, low power consumption and higher switching frequency than transistor founded technology. The code converters are the basic unit for transformation of data to implement arithmetic processes. In this work, QCA created 4-bit binary-to-gray code converter have been planned. The planned design decreases the number of cells, area and increases switching speed. The simulations are completed using QCA Designer and Microwind tool which is extensively used for simulation and verification.

Keywords: Binary to Gray Converter,Quantum Dot Cellular Automata(QCA), QCA Cell, Complementary Metal-Semiconductor(CMOS), Microwind, Design Schmetic(DSCH).

1. INTRODUCTION

QCA is aprogressiveadmittanceheaded for the modern period of nanotechnology and substitutes of CMOS technology [1] and proposals a novel designing method which is relevant for logic gates. Physical bounds of CMOS such as quantum possessions and technological limits like power dissipation; hamper the momentum of microelectronics by regular circuit mounting [2]. QCA is adeveloping technology which permits operating frequencies in range of THz [3] that is not realizable in current CMOS technologies. Renovation circuit embedded between dual structures if each uses diverse codes for the similar information. Conventional CMOS has conquered our fabrication trade for last few decades and it has showed to be an improvedsubstitute than earlier technologies but very soon a day will come when our conventional CMOS technology of device scheming will reach its restriction and we will have to travel to a new technology. Quantum Dot Cellular Automata demonstrations all signs of becoming commanding and better substitute to Conventional CMOS Technology. In the year 1993 C S Lent presented Quantum Dot Cellular Automata and in the year 1997 QCA was physically confirmed [1]. CMOS Technology is inflexible to promotion further because of boundaries posed by short channel effect and ever diminishing size of gate oxides at NanoScale. A code converter is a combinational circuit which produces two structures dependable even each uses distinct binary code. In this paper we have planned and executed a 4-bit binary-to-gray code converter in QCA technology and associate the optimum design to the CMOS Binary to Grey design. Executed proposed binary to gray converter in an effective way

2. QCA PRELIMINARIES

In this segment, the building unit i.e. QCA cell, general logic, and gates in QCA are examined in the order of QCA cell, QCA wires, majority gates, inverter, AND-OR gates.

2.1 QCA cell

The embryonic cell in QCA technology, as shown in Fig.1 (a), is a square-shaped cell.It comprisesfour quantum dots at each corner of the cell. The quantum dot normallycomprises two electrons in each cell, which occupy two dots of the cell. Due to the Columbic repulsion between the electrons, the electrons tend to lodge the location which has lower repulsion force between them and electrons can occupy steady states. Hence, they inhabit the slanting position within the cell. There are two approaches possible for the placement of electrons as shown in Fig.1 (b). Thus, two polarities are possible. If the electrons lodge the position as shown in Fig.1 (b) then it corresponds to polarization "1" i.e. logic 1 and if is decided as shown in Fig.1(c) then it is in polarization "-1" i.e. logic 0 states. These 2 extra mobile electrons can quantum mechanically tunnel among dots, but not cells. Hence different conventional digital circuits in which information is approved by the flow of electric current, QCA functions by the Columbiccontact that connects the state of one cell to its neighbor cell state.
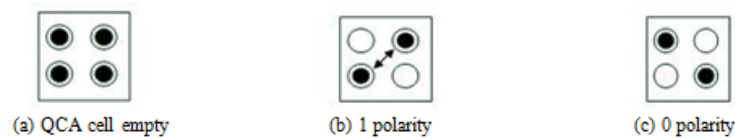

(a) QCA cell empty   (b) 1 polarity   (c) 0 polarity

Fig.1 QCA cell

2.2 QCA wire and types

In imperative to conduct the information from one cell to another, a QCA wire is desirable. The wire contains of a chain of cells where the cells are also attached to each other. The logic values are accepted from one cell to the next cell due to the coulomb collaboration. The polarization of the input cell is covered down the wire. As a result, the arranged system effort to settle down to a ground state. Due to electron repulsion if the polarization of one cell variations, it enforces its next to cells to change its state as shown in Fig.2.

Cells 2-9 have lower potential barriers

Cell 1 = Input cell   Cell 2 switches its polarization due to Coulombic interaction

Fig.2 QCA Wire

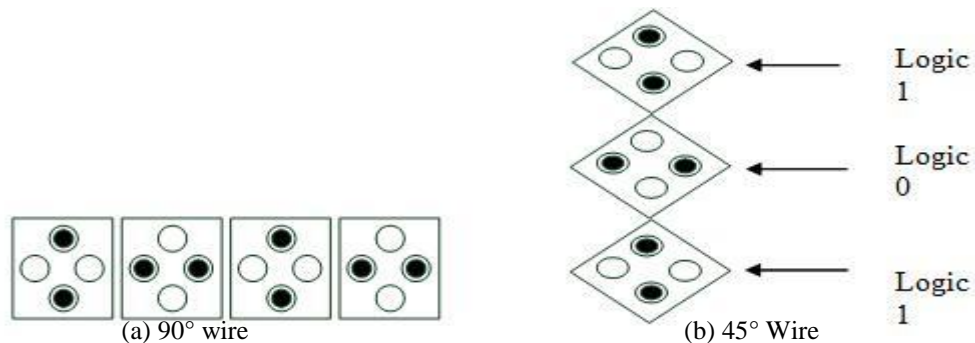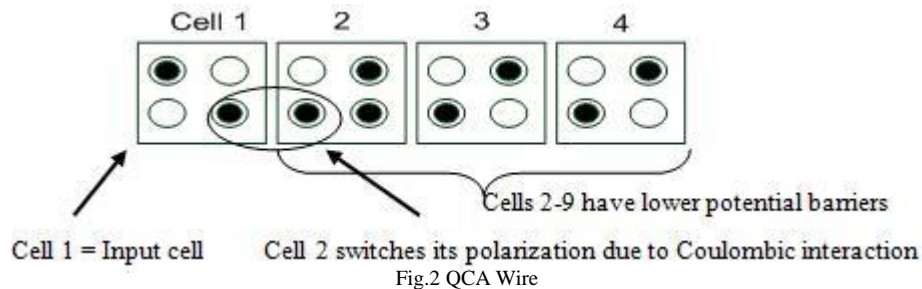(a) 90° wire   (b) 45° Wire

Fig.3   QCA wire types

The manner of retaining quantum dot in the square cell makes it probable to have two styles of orientation. The first is called as 90° wire and the another is 45° as shown in Fig.3(a) and 3(b) in which each other cell with conflicting polarity is put together.

2.3 Majority gate

Majority gate is one and only of the fundamental gates of QCA. It is shown in Fig.4 which is a 3-input majority function. The output is solely the majority of the 3 inputs applied. Supposing the inputs is A, B, and C, the Boolean function of the majority gate is,

$$M (A, B, C) = AB+AC+BC \tag{1}$$

Now if we dose the polarization of one input to logic "0", say B, then equation (1) can be associated as follows:

$$M (A, 0, C) = A.0+AC+0 = AC \tag{2}$$

Hence equation (2) is basically the AND operation between A and C input. Similarly if we put the input B value equivalents to "1" then,

$$M (A, 1, C) = A.1+AC+1.C = A+C+AC = A (1+C) +C = A+C \tag{3}$$

Equation (3) is an OR procedureamong A and C. Consequently by changing the worth of any of the input, the 3-input majority gate can function as AND gate and OR gate.
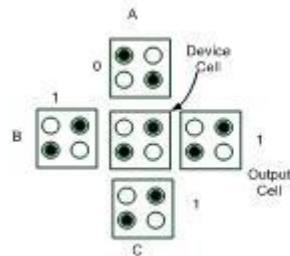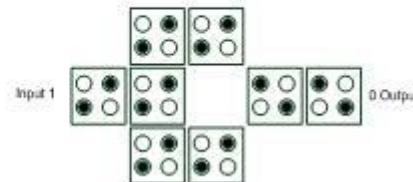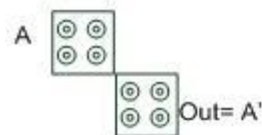

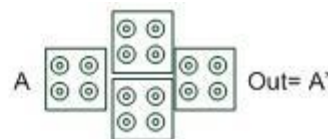Fig.4 Majority Gate Structure [9]   Fig. 5 (a) Inverter

2.4 Inverter gate

There are numerous ways to do it in the QCA standard that one is shown in Fig.5.In fig. (a), the signal originates from the left, ruptures into two parallel wires, and is inverted at the point of convergence [1]. The additional arrangement used to make inverter chain as shown in Fig.5 (b) and 5 (c).

(b)   (c)

Fig.5 (a), (b), (c) Three alteredstyle inverter in QCA

However, assignment of two cells such that they slant via only one corner leads to switch from -1 logic to +1 logic or vice versa as shown in Fig.5(b).

2.5 QCA clocking scheme

In VLSI design, the purpose is organized by a clock signal which is characteristic to the technology used. In divergence to this, QCA exhibit clocking scheme as the most necessary concept to understand. As we know there is no flow of any current indicator in the propagation of information in QCA, this does not really means that power dissipation must be zero. Clocking in QCA not only deliberate control of information flow but also true power gain in QCA [7]. The signal energy pay for to the environment is reinstated by the clock used. Clocking in QCA is skillful by two types of switching approaches for its operation: abrupt switching and adiabatic switching. In abrupt switching, the inputs changes suddenly and the circuit can be in some excited state; subsequently, the QCA circuit is undisturbed to ground state by dissolving energy to the environment [11]. This inelastic relaxation is ungoverned and the QCA circuit may inscribe a metastable state that is reasoned by a local, rather than a global energy ground state. Therefore, adiabatic switching is usually favored; in adiabatic switching, the system is continuously kept in its prompt ground state [11]. After smearing the clock signal, the electrons may either lacking to the four corner dots or pull them into the two intermediate dots. When the electrons are in the middle dots, the cell is supposed to be in the "null" state and when the electrons are in the four corner dots, the cell is in lively state. The cell in an active state is used to signify binary "0" and "1" values as shown in fig.1. This clocking arrangement (which was suggested in [7] consists of four phases: Switch, Hold, Release, and Relax, as shown in Fig.6 (a).

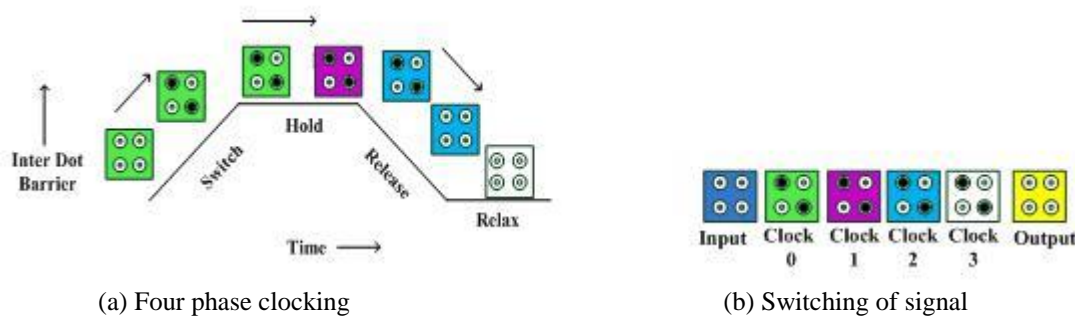(a) Four phase clocking   (b) Switching of signal

Fig.6 Clocking in QCA

All cells in a region are measured by the same clock signal. Cells in each zone achieve a specific calculation. During the Relax phase, the electrons are dragged into the middle dots, and the cell is in "null" state. During the Switch phase, the interdot barricade is easy raised and shoves the electrons into the corner dots, so the cell obtains a conclusive polarity under the supremacy of its fellow (which are in the Hold phase). The operation of fig.6 (b) is summarized below:

- Through the first clock phase, the switch phase, the inter-dot potential barricades are low. The barriers are then elevated during this phase and the QCA cells become polarized rendering to the state of their driver (i.e. their input cell).It is in this clock phase that the actual calculation occurs. By the end of this clock phase, barricades are high enough to conquer any electron tunneling and cell states are immovable.
- During the second clock phase, the hold phase, barricades are held high so the outputs of the sub-array can be used as inputs to the next stage.
- In the last clock phase, the release phase, barriers are depressed and cells are allowed to decrease to a unpolarized state.

Finally, during the fourth clock phase, the relax phase, cell barricades remain lowered and cells continue in an unpolarized state

3. PROPOSED CIRCUIT AND PRESENTATION

The enormousaccessibility of codes for corresponding dissimilar elements of information outcomes in the use of discrete codes by discretepatterns and it is prerequisite sometimes to use the result of the one system as engaged to the input to another system. Code converters are circuits that convert a code into one more which is programmed in logic arrays and recycled in many fields such as defensive information from third events and increase data flexibility. It is also effective in safety department for devising and cracking codes.

3.1 Binary code

A code is a representative presentation of data and achieves text information using the number system. For occurrence a binary sequence of six bits 110100 is identical to decimal number 52.
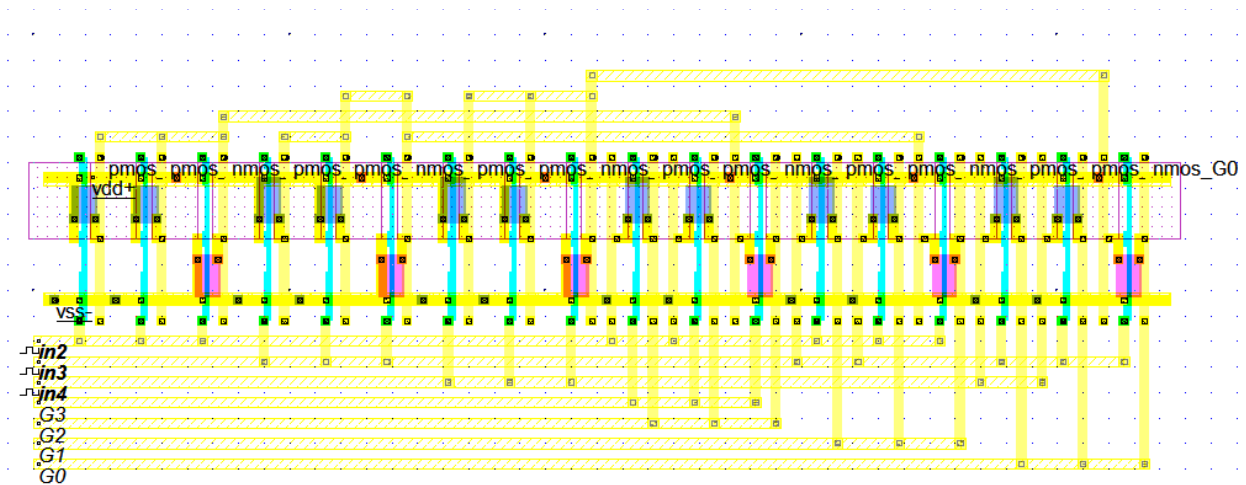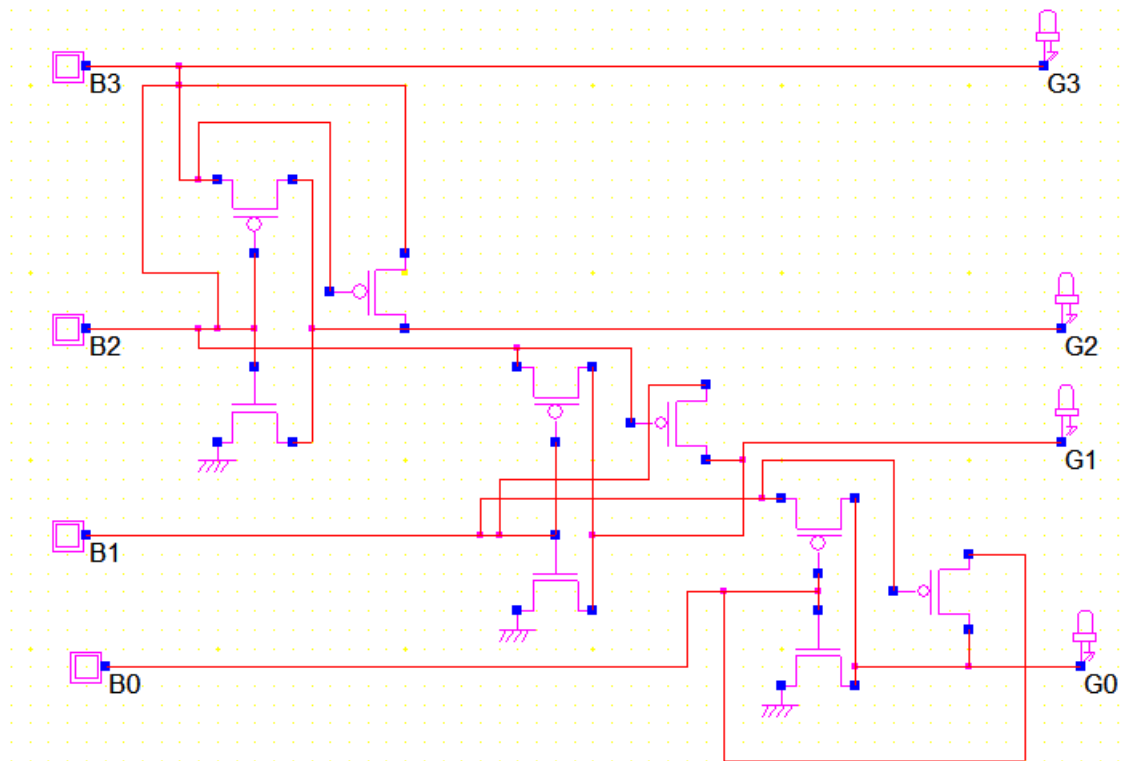
3.2 Gray code

Reproduced binary code, also recognized as Gray code is a numeral arrangement where each charge varies only a sole bit from the previous bit. Gray code is not suitable for arithmetic operations. Gray code has many beneficial applications including abridge fault correction, terrestrial television, some cable television system, analog-to-digital converter and peripheral device.

3.3 CMOS Binary To Gray Code Converter

Numerous digital systems uses diversity of codes for the same information contented. So occasionally it becomes essential to feed the response of one system to the input of additional. Therefore, change unit must be reserved between two systems. A code converter circuit brands the systems well-matched even if those systems usedissimilar codes. In telecommunication and computing, binary codes are used for a numerous methods of encoding data such as character strings, into bit strings. In general binary coding is done by transmission sequence of strings in the form of 0s and 1s corresponding to data inputs.

In Gray code consecutive number differs by only 1 bit and hence it is also well-known as unit distance code. It is also named cyclic code or reflective code. A stimulating application for Exclusive-OR gate is a logic circuit to change a binary number to its comparable in Gray code and vice versa. A conservative binary to Gray code converter is shown in Fig. 10. It consists of three XOR gates in a waterfall fashion. Since XOR gates using CMOS methodneeds a large number of transistors, this method is not practicable in compound circuits. Hence there are few more methods that offer healthierpresentation which can be careful to perform this code conversion. PTL is another method that can be accepted to realize conservative code converters. But because of the abridged output swing, other methods like GDI and MGDI need to be booked under consideration. Other power reduction methods are also intentional [7].

Fig. 7 CMOS implementation of Binary to Gray code

Fig.8. Layout of Binary to grey Converter

4. QCA IMPLEMENTATION OF BINARY TO GREY CODE CONVERTERS

Figure 9 shows the basic block diagram of 4-bit binary-to-gray code converter using majority voter. Four bit binary-to-gray code converter collected of 4-inputs B3, B2, B1 and B0 and the conforming gray outputs are G3, G2, G1 and G0.Tables 1 to 3 shows the truth table of binary-to-gray code converter
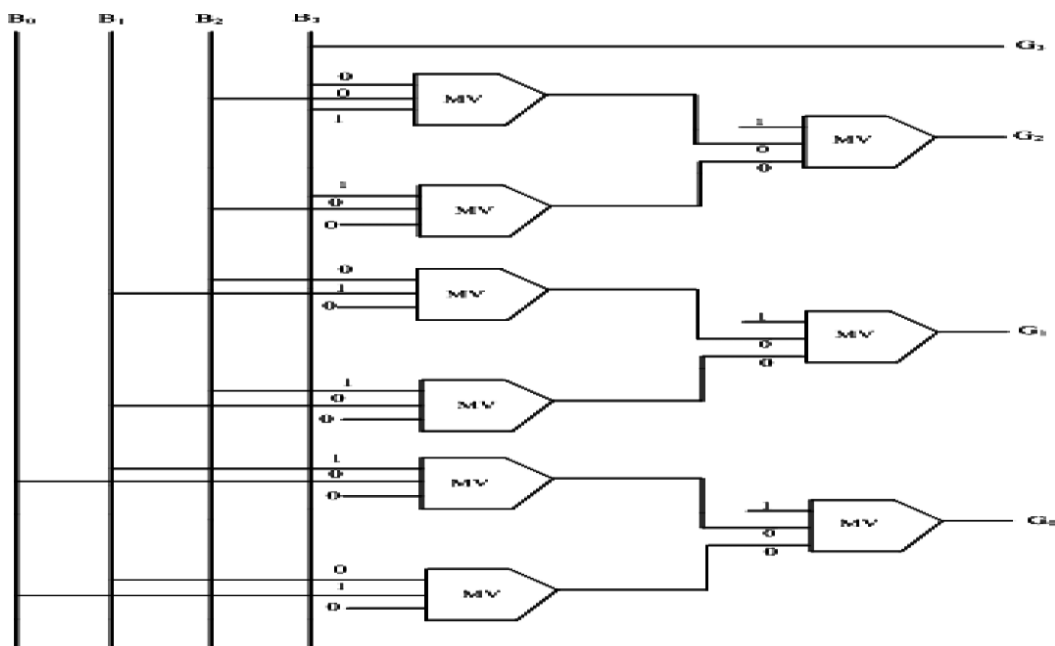

Fig. 9 Block Diagram of Binary to grey converter

Table 1: Truth table Representations of four bit Binary to Gray Code Converter.

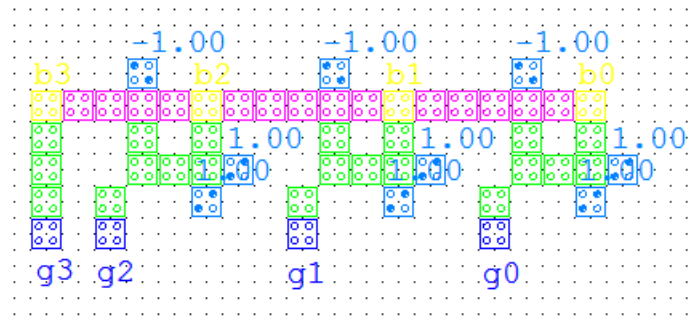| Binary Inputs				Gray Outputs			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

5. SIMULATION AND RESULTS

Fig.10. QCA implementation of Binary to Grey Converter
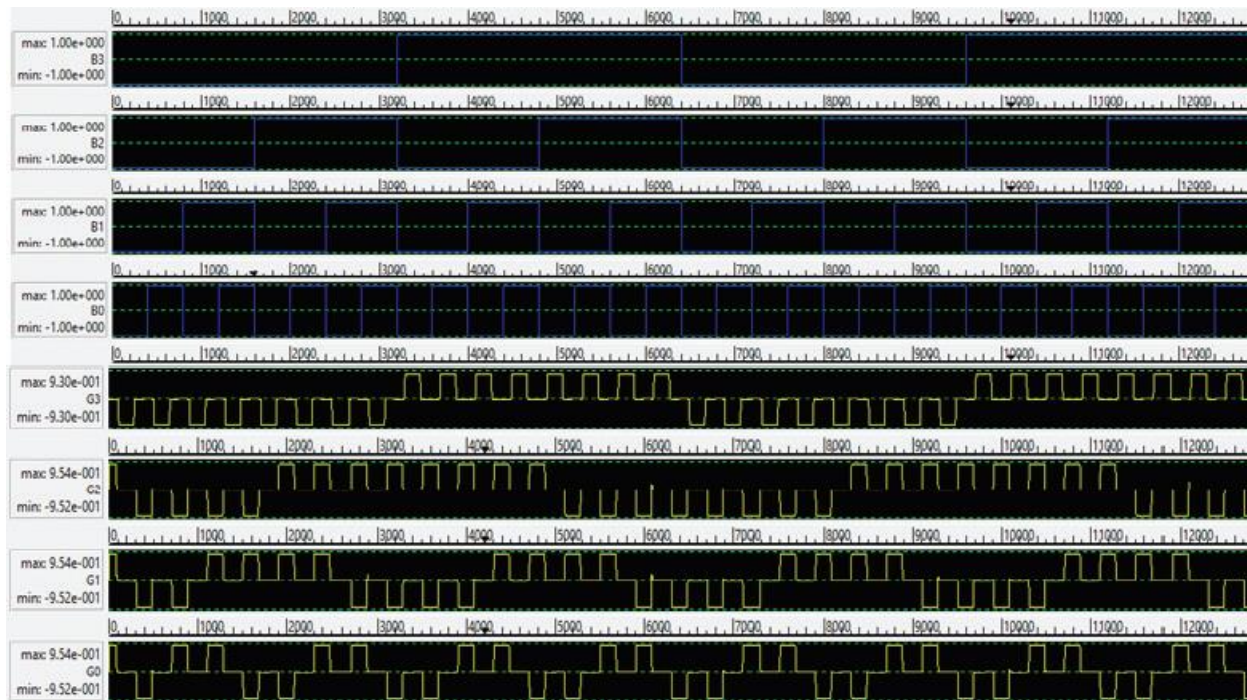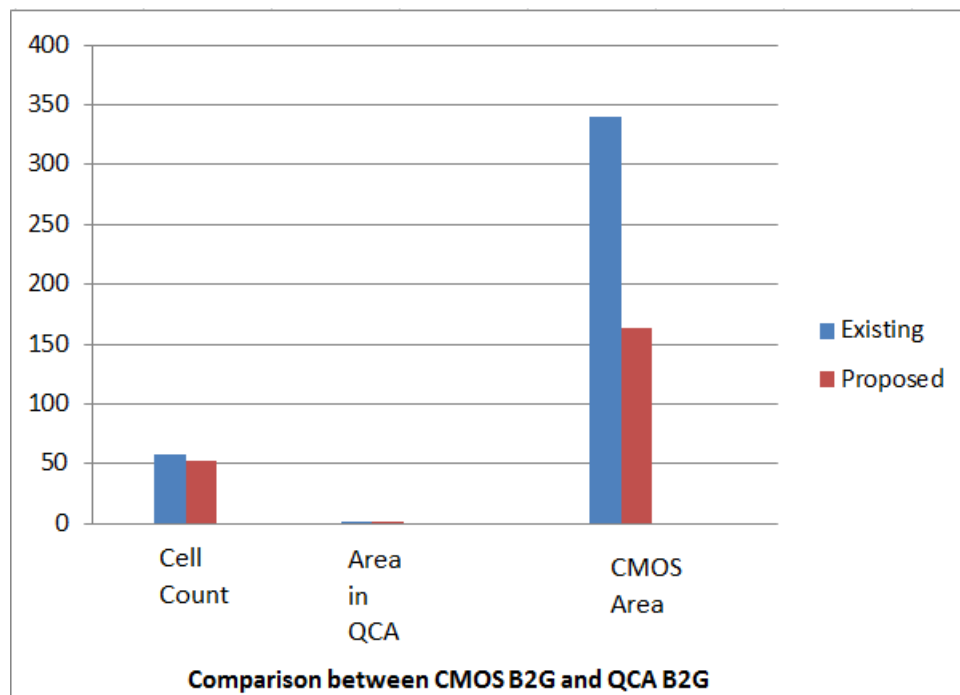

Fig.11. Simulation Output of Binary to Grey Converter

Table 2: Performance Factors of Binary to Gray Code Converter.

Parameter	Proposed4 bit B2G	Existing 4 bit B2G
Total Number of Cells	52	58
Number of Clock	2	3
Clock delay	0.75	1
Area in QCA (μm2)	0.07	0.08
Area in CMOS (μm2)	163(using GDI)	339.82

Comparison between CMOS B2G and QCA B2G

6. CONCLUSION

In this paper, the project and simulation of QCA binary to grey code converter circuits has been obtainable. The operation of these converters has been scrutinized using QCA designer bi-stable vector simulation. The designs are proficient where it comprises less number of cells, use minimum clock phases and have meaningfully minimum wire length which origins to trouble-free operation at advanced temperature. The projected converter has an advantage in terms of number of cells (47% for 4-bit) from an earlier circuit proposed by [6].

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