DESIGN AND ANALYSIS OF SRAM ARRAY ARCHITECTURES

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Abstract - Memory architecture describes the method used to implement Electronic computer data storage in a manner that is a combination of the fastest, most reliable, most durable and least expensive way to store and retrieve information. Memories are the crucial part of any digital system and probably no digital system can be completed without memories. Compact devices and embedded systems are emerging, so the low power consumption is very essential to the architectural design. As microprocessors and other electronic applications get faster and faster, the need for large quantities of data at very high speeds increases. Multiple assist schemes and design strategies will be used to increase the stability of memory cells as the role of these assist schemes is to help in achieving a robust read or write operation. This project will present the complete design of SRAM sub-system architecture. And the design will be simulated and analyzed by using PYXIS TOOL from Mentor Graphics at 130nm technology

Index Terms – **Static Random Access Memory (SRAM), Memory Architecture, Mentor Graphics, Pyxix Tool.**

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I.   INTRODUCTION

Fast & low power SRAMs are becoming the main component in many VLSI chips. Mainly SRAMs are used in cache memories. SRAMs are designed to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in system that requires very low power consumption. In several applications, the embedded SRAMs can occupy the larger chip area and contain hundreds of millions of transistors. SRAMs need to be not only fast but also reliable, i.e., it must be stable and robust to the system work properly.

The main objective of this work is to design a complete SRAM architecture using 130 nm technology. All architectures are composed by five circuits: Bit cell, Sense amplifier, Pre-charge, Write driver & Decoder.

Use of SRAM:

Design tradeoffs will include speed, volatility, cost, and many other features. All these factors should be considered before the selection process of a RAM for designing our system. Let us discuss all these factors in brief:
   • Speed:
      The primary and the foremost advantage of an SRAM over DRAM is its speed. The fastest DRAMs on the market still require more than five processor clock cycles to access the first bit of data.
   • Volatility:
      SRAM cannot hold the data if the power is removed. The SRAM cells do not need to be refreshed like DRAM. SRAM supports faster read and write times than DRAM.
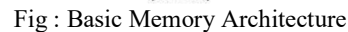   • Cost:
      If cost is the major factor in a memory design, then DRAMs will be the low cost instead of SRAM. The performance is a critical factor then using a well designed SRAM is an effective and cost performance solution for us.

II.   MEMORY ARCHITECTURE

Memory Architecture describes the methods used to implement data storage in a manner that is a combination of the fastest, most reliable, most durable, and least expensive way to store and collect the information.

   The data storage structure, consists of individual memory cells arranged in an array of horizontal rows and vertical columns. Each cell is capable of storing 1-bit of binary information. In this structure, there are 2N rows also called word lines and 2M columns also called bit lines.

   Thus, the total number of memory cells in this array is given as 2N x 2M. To access a particular memory cell, i.e., a particular data bit in this array, the corresponding word line and corresponding bit line must be selected according to the address coming from the outside of the memory array.

Fig : Basic Memory Architecture

The main SRAM building blocks include various components. All these components or blocks used in the SRAM are listed as follows:

• SRAM cell
• Pre-Charge Circuit
• Write Driver circuit
• Sense Amplifier
• Row decoder

SRAM CELL

The SRAM data storage cell, i.e., the one-bit memory cell consists of a two inverters connected back to back in a simple latch circuit with two stable operating points. Depending on the state of the two inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '0' or as logic '1'.

An SRAM cell has three different states it can be in: standby when the circuit is idle, reading when the data has been requested and writing when updating the contents. When SRAM is operated in read mode should have read- stability and in write mode should have write-ability.

Fig : Schematic Of SRAM Cell

PRE-CHARGE

The pre-charge of the bit lines is a very important factor for the correct functioning of the SRAM. To perform the read operation it is necessary that the bit lines are charged at the same voltage. After the writing and reading operations, one of the bit lines is discharged generating an undesired voltage difference between the bit lines. After these operations, the pre-charge circuit has the function to equalize the bit lines voltages to the supply voltage.
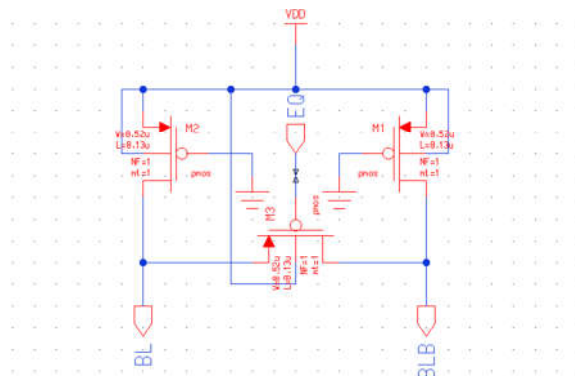
Fig : Schematic Of Pre-charge

SENSE AMPLIFIER

The sense-amplifier (SA) plays a major role in SRAM architecture. During the read operation one of the bit lines discharges while the other bit line remains at supply voltage. This slow discharge is due to the large bit line capacitance and the access transistor of the bit cell is small. For this reason, the SA is used to amplify a small difference between the bit line voltage values to digital levels. The SRAM performance during the read operation is improved due to the Sense - Amplifier circuit. The most common types of SA are Cross coupled sense amplifier, Latch type sense amplifier, Current mirror sense amplifier. The Current mirror SA was chosen as the read circuit for this work.
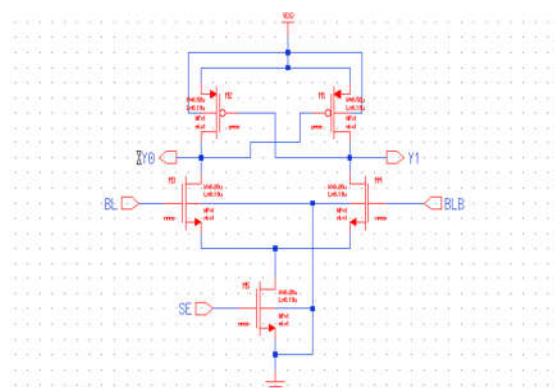
Fig : Schematic Of Sense Amplifier

WRITE DRIVER

The Write Driver is responsible for writing a specific value in the bit-cell. The circuit has the function of charging or discharging the bit lines to the desired bit be written in the memory cell. The circuit schematic of write driver designed in this work is presented in below figure.

This circuit has two input signals, they are the signal representing the bit value to be written in the memory cell, and the control signal write enable (WE). The control signal WE function is to allow or not the access to the bit lines by the Write Driver. When WE is on, the Write Driver imposes in the bit lines the required voltage values for writing the desired value in the Bit-Cell.
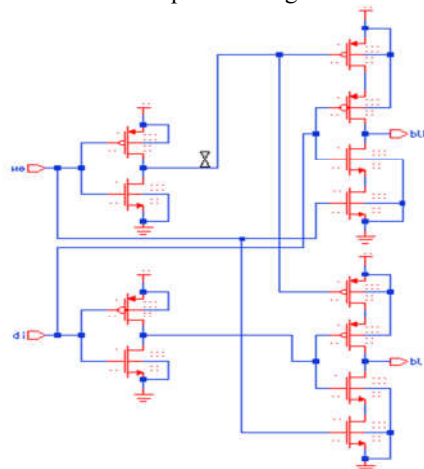
Fig : Schematic Of Write Driver

DECODER

In digital electronics a binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs. They are used in a wide variety of applications including data demultiplexing, seven segment displays, and memory address decoding.

There are several types of binary decoders, but in all cases a decoder is an electronic circuit with multiple input and multiple output signals, which converts every unique combination of input states to a specific combination of output states. In addition to integer data inputs, some decoders also have one or more "enable" inputs. When the enable input is negated (disabled), all decoder outputs are forced to their inactive states.

The row decoder selects one of those rows, depending on the N-bit address given to it. The column decoder selects a particular column in the memory array for reading the contents of the selected memory cell or to modify its contents.
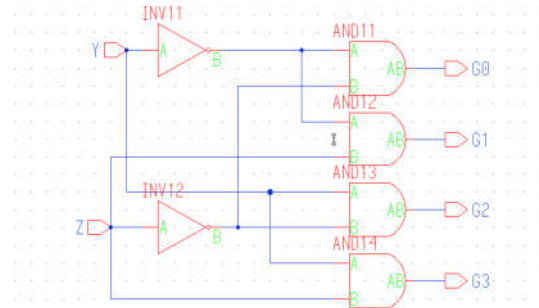

Fig : Shematic Of Decoder

III. DEVICE PARAMETERS

Static Noise Margin (SNM):

The SRAM cell immunity to Static Noise is measured in terms of SNM, that qualifies the maximum amount of noise voltage that can be tolerated at the cross coupled inverter nodes without flipping the output data or the cell data. when the bit lines are pre charged to high voltage then only the SNM can be plotted while reading the data from the cell.

Read Static-Noise-Margin(RNM):

During read accesses, the Read-SNM decreases. This is due to the reason that Read-SNM is calculated when the word line is set high and both bit line are still pre charged high. At the onset of a read access, the access transistor (WL) is set to "1" and the bit-lines are already pre-charged to "1".The internal node of the bit-cell representing a zero through the access transistor due to the voltage dividing effect across the access transistor and drive transistor. This increase in voltage severely degrades the SNM during the read operation as shown in the Figure.

Write Static-Noise-Margin(WNM):

The write noise margin is defined as the minimum bit line voltage needed to flip the state of cell. During a write operation, the input data are sent to the bit lines, and then the word lines are activated to access the cell. The bit line that is charged to '0' pulls the node of the cell storing '1' to '0' causing the cell to flip state.
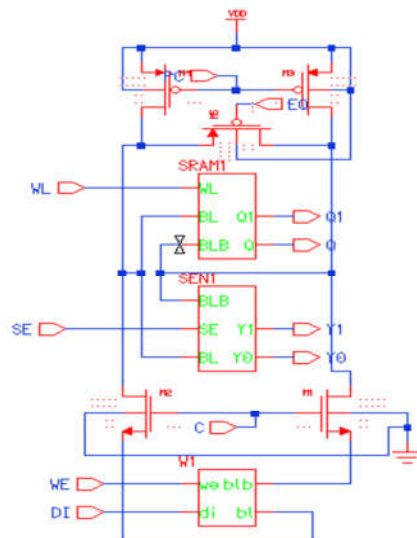
1 BIT MEMORY ARCHITECTURE

Fig : Schematic Of 1BIT Memory Architecture
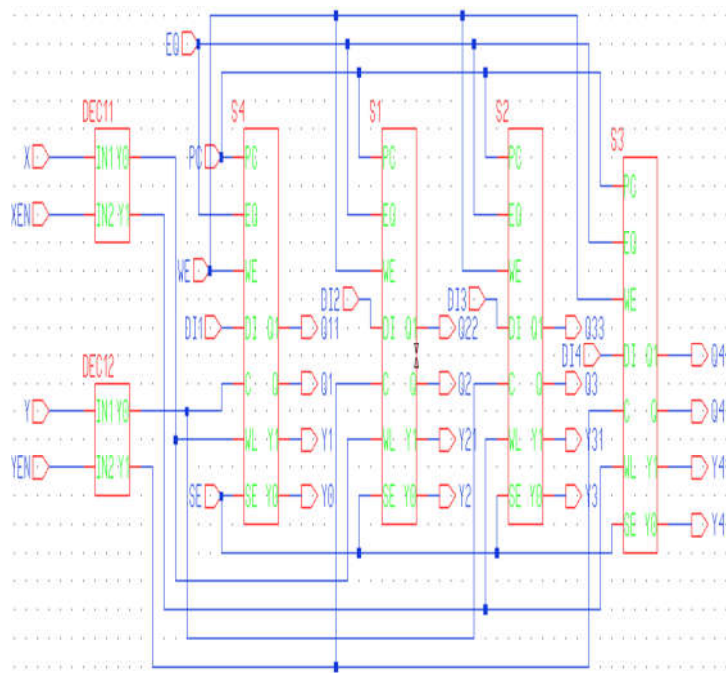
4 BIT   MEMORY ARCHITECTURE

Fig : Schematic Of 4 BIT Memory Architecture
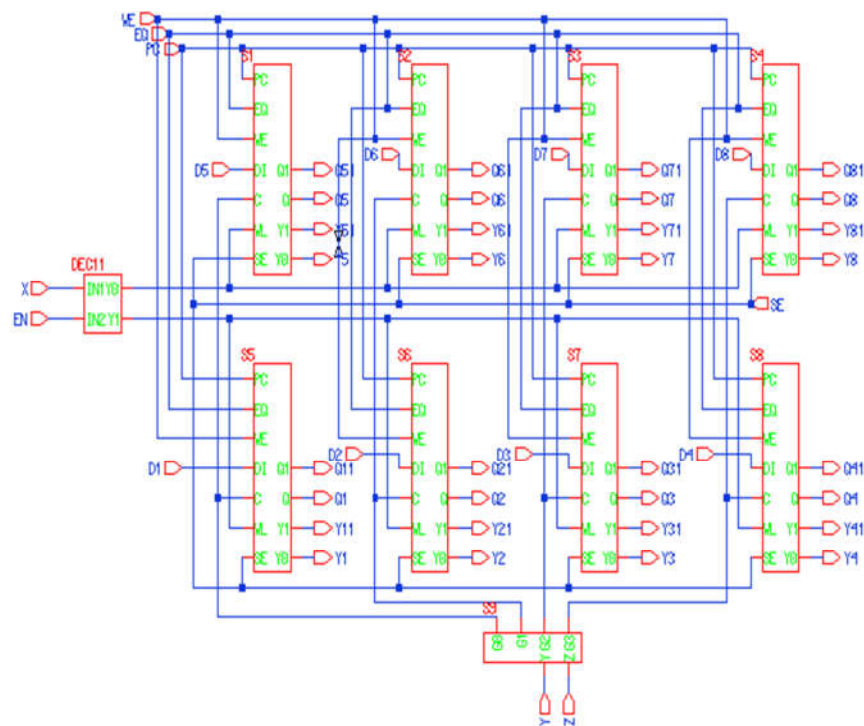
8 BIT MEMORY ARCHITECTURE

Fig : Schematic Of 8 BIT Memory Architecture
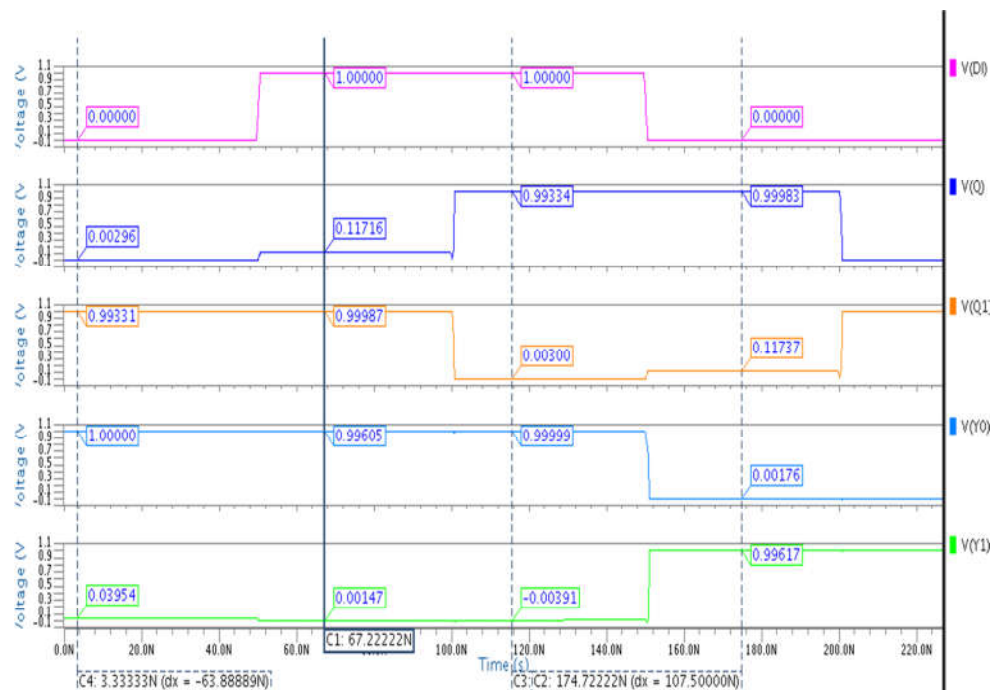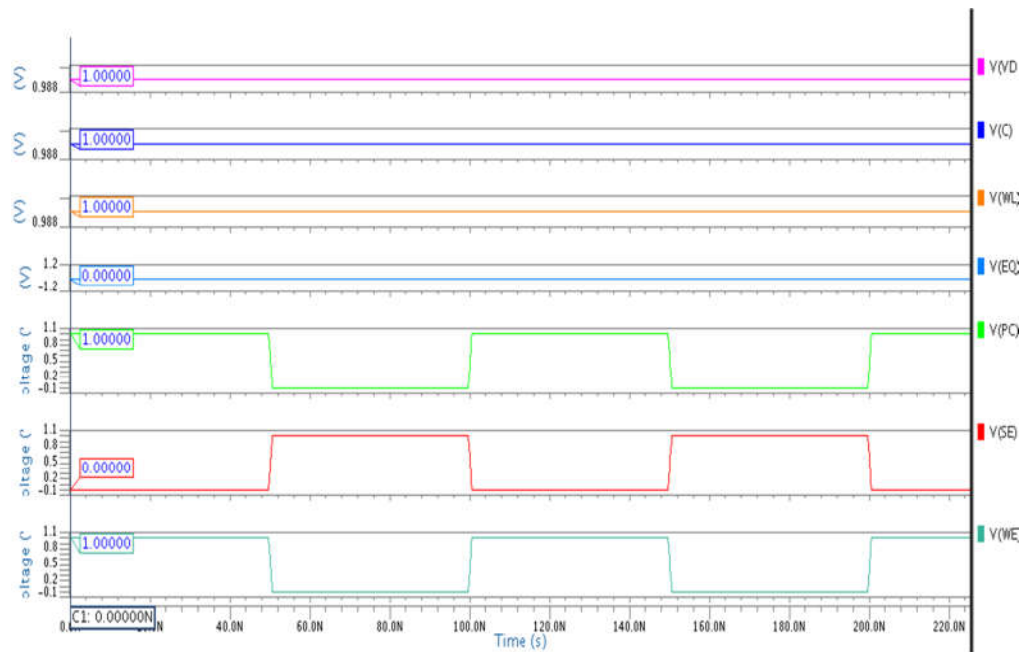
SIMULATION RESULTS

Fig : Output Waveforms Of 1 BIT Memory Architecture

IV. RESULT ANALYSIS

SRAM Architectures		Write Noise Margin (WNM)	Read Noise Margin (RNM)	Power Dissipation (Watts)
1 BIT	Bit 0	0.00300	0.00176	2.6316U
	Bit 1	0.00665	0.00383	
4 BIT	Bit 0	0.004	0.00147	19.8727U
	Bit 1	0.00669	2.95629M	
8 BIT	Bit 0	2.95816M	1.45540M	50.4183U
	Bit 1	0.00669	0.00039	

V. CONCLUSION

The schematics of different architectures are designed and analyzed in Pyxis tool and ELDO simulator from mentor graphics at 130nm technology.

In this project, we designed different sizes of SRAM Memory architectures and obtained various parameters like read noise margin (RNM), write noise margin (WNM), Power Dissipation (PD).

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