# HDL Implementation of Digital Image Enhancement

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Abstract- Digital image processing is an ever expanding and dynamic area with applications reaching out into everyday life such as medicine, space exploration, surveillance, authentication, automated industry inspection and many more areas. Applications such as these involve different processes like image enhancement and object detection. Implementing such applications on a general purpose computer can be easier, but not very time efficient due to additional constraints on memory and other peripheral devices. Hardware implementation for application specific can offer much greater speed than a software implementation. With the advancement in the Very Large Scale of Integration (VLSI) technology hardware implementation has become an attractive alternative. Implementing complex computation tasks on hardware and by exploiting parallelism and pipelining in algorithms yield significant reduction in execution times. It has been observed that most of the work has been done either in C and JAVA. No work has been done in the VHDL to design and develop the chip for image enhancement algorithms. Intensity transformation is used to enhance the size of image pixels. The chip design for 2D and 3D image enhancement is done in Xilinx 14.2 software. Image enhanced values are verified with the help of waveform editor of ISE Simulator.

#### I. INTRODUCTION

Digital image processing is electronic data processing on a 2D array of numbers. An image is represented with 2D array. Image processing techniques are used to modify pictures and improve the quality with the different techniques such as enhancement, restoration, extract information analysis, recognition, and changing their structure composition[7][8], image editing. Images can be processed by photographic optical and electronic means, but image processing using digital computers is the most common method because digital methods are precise, fast and flexible. An image can be synthesized [8] from a micrograph of various cell organelles by assigning a light intensity value to each cell organelle. The sensor signal is "digitized" converted to an array of numerical values, each value representing the light intensity of a small area of the cell. The digitized values are called picture elements, or "pixels," and are stored in computer memory as a digital image. A typical size for a digital image is an array of 512 by 512 pixels, where each pixel has value in the range of 0 to 255. The digital image is processed by a computer to achieve the desired result. Image enhancement improves the quality of images for human viewing. Removing blurring and noise, increasing contrast, and revealing details are examples of enhancement operations [2][13]. For example, an image might be taken of an endothelial cell, which might be of low contrast and somewhat blurred. Reducing the noise and blurring and increasing the contrast range could enhance the image. The original image might have areas of very high and very low intensity, which mask details. An image enhancement uses adaptive algorithms adjust their operation based on the image information pixels being processed. In this case the mean intensity, contrast, and sharpness could be adjusted based on the pixel intensity statistics in various areas of the image. Image processing technology is used by planetary scientists to enhance images of Mars, Venus, or other planets. Doctors use this technology to manipulate CAT scans and MRI images [8] [2]. A graphical display can be improved with the image features enhancement such as boundaries, or contrast. It includes contrast level & gray manipulation, edge crisping, noise reduction, and sharpening, filtering, pseudo coloring, interpolation, magnification and so on. Image enhancement deals with the improvement of visual appearance of the scene, to improve the detect ability of objects to be used by either a machine vision system or a human observer. Integrated image capture,

processing, and communication power on a compact, portable, hand-held device is attracting increased interest from computer vision researchers with a goal of applying a diverse collection of vision tasks on the small hand-held device. The research emphasis on computer vision to pattern enhancement technologies and the chip implementations that can be used in camera phones, mobiles, scanners etc.

#### **IMAGE ENHANCMENT METHODS**

The 2D image I is ordinarily represented in software accessible form as an  $M \times N$  matrix containing indexed elements I(i, j), where . The elements I(i, j) represent samples of the image intensities, usually called pixels .For simplicity, assume that it come from a finite integer valued range. Image enhancement techniques can be divided into two broad categories Spatial domain methods Which operate directly on pixels, and Frequency domain methods Which operate on the Fourier Transform of an image.

## 2.1 Spatial Domain Methods

The value of a pixel with coordinates (x, y) in the enhanced image is the result of performing some operation on the pixels in the neighborhood of (x, y) in the input image, F. Neighborhoods can be of any shape, but usual form is rectangular.

## 2.1.1 Grey scale manipulation

In gray scale manipulation the operator acts on a 1x1 pixel neighborhood in the input image, that is (x,y) only depends on the value of F at (x, y). This is a grey scale transformation or mapping. The simplest method is thresholding where the intensity profile is replaced by a step function, active at a chosen threshold value. In this case any pixel with a grey level is the threshold in the input image gets mapped to 0 in the output image. Other pixels are mapped to 255. Different types of grey scale transformations are shown in figure 1.



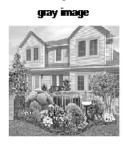
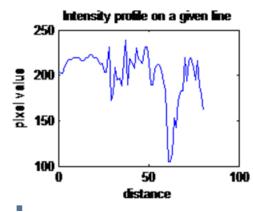


Fig.1. Gray Image Conversion

## 2.1.2 Histogram Equalization

Histogram equalization is a common technique for enhancing the appearance of images. Consider an image which is predominantly dark. Then its histogram would be skewed towards the lower end of the grey scale and all the image detail is compressed into the dark end of the histogram. It is possible to stretch out the grey levels at the dark end to produce a more uniformly distributed histogram then the image would become much clearer. Histogram equalization involves finding a grey scale transformation function that creates an output image with a uniform histogram.





## 2.3. Image Enhancement Techniques

Image Enhancement Techniques are listed below Contrast Enhancement Method Smoothing of an Image. Brightness Threshold Intensity Transformation 2.3.1 Contrast Enhancement Method An Image is taken and its contrast is

increased or decreased as per the enhancement requirements of the Image. The required contrast enhancement is achieved applying the Histogram Stretching of the Image. 2.3.2 Smoothing A noisy Image is taken and the noise removal is done by applying a smoothing technique. The noise removal is achieved by using a mask which enables neighborhood pixel processing. The aim of image smoothing is to diminish the effects of camera noise, spurious pixel values, missing pixel values etc. There are many different techniques for image smoothing, but neighborhood averaging and edge-preserving smoothing are suiting to our application. Neighborhood Averaging [13], is an approach in which each point in the smoothed image, (x,y) is obtained from the average pixel value in a neighborhood of (x,y) in the input image. For example, use of a 3 x 3 neighborhood around each pixel masking is done.

Each pixel value is multiplied by 1/16, summed, and then the result placed in the output image. This mask is successivelymoved across the image until every pixel has been covered. Edge preserving smoothing, Neighborhood averaging or Gaussian smoothing will tend to blur edges because the high frequencies in the image are attenuated. An alternative approach is to use median filtering. Setting of the grey level is done to be median of the pixel values in the neighborhood of that pixel. The median m of a set of values is such that half the values in the set are less than m and half are greater. For example, suppose the pixel values in a 3 x 3 neighborhood are (10, 20, 20, 15, 20, 20, 25, and 100). With the help of sorting technique among the values (10, 15, 20, 20, |20|, 20, 20, 25, 100) median value is found 20.

original image A



complement of image A



original image B



complement of image B



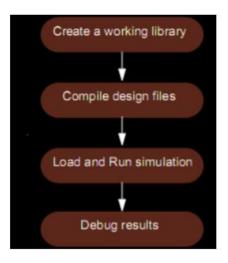
### 3. TOOLS & HDL ENVIRONMENT

Project navigator Application Version ISE 14.2 of Xilinx Company: Xilinx [11] has been a semiconductor industry leader at the forefront of technology, market and business achievement. It is a tool to design the IC and to view their RTL (Register Transfer Logic) schematic. It is a tool to test the code on FPGA environment and we can get the all parameters details required to implement the Chip. ModelSim EE 10.0 D of Mentor Graphics Company: Mentor Graphics was the first to combine single kernel simulator (SKS) technology with a unified debug environment for

Verilog, VHDL, and System C. The combination of industry leading, native SKS performance with the best integrated debug and analysis environment make ISE [12] the simulator of choice for both ASIC and FPGA design. The best standards and platform support in the industry make it easy to adopt in the majority of process and tool flows. Simulation and Design Steps The following diagram shows the basic steps for simulating a design in Xilinx.

## III. Advantages of FPGA

- Better performance than DSP's
- > Less Time to Market
- ➤ Low long-term Cost
- ➤ More Reliability
- ➤ Long-term Maintenance



#### 4. SIMULAION RESULTS

The result obtained in Modlesim software for image enhancement chip is shown below in figure. Step input 1: reset =1, clk is used for synchronization and then run. Step input 2: reset =0, same clk is used for synchronization, give image input value and scaling value to get the results. We have taken the case of

Image image\_in (x), image\_in (y) have the discrete instant values and sample\_in(x) and sample\_in(y) are the value which should be added resulted values are image\_out(x) and image\_out(y). The result obtained in Modlesim software for image enhancement chip is shown below in figure. Step input 1: reset =1, clk is used for synchronization and then run. Step input 2: reset =0, same clk is used for synchronization, give image input value and scaling value to get the results. We have taken the case of 3D Image image\_in (x), image\_in (y) and image\_in (z) have the discrete instant values and sample\_in(x), sample\_in(y) and sample\_in(z) are the value which should be added resulted values are image\_out(x), image\_out(y) and image\_out(y).

# 4.1 Device utilization & Timing Summary of 2D and 3D image

Device utilization is the hardware and logic circuitry required to implement the design. It consist of no. of slices, flip flops, gates, combinational logic circuitry and input/output blocks.

Selected Device: 3s400pq208-4

Table 1 Hardware utilized for image enhancement chip

FPGA	2D chip
Resources	
Slices	45,23%
Slice	43%
Registers	
LUTs	15.7%
IOB	15%
GCLKs	25%

Equivalent	227,176
Gate Count	

# **4.2 Timing Summary**

Timing summary is the detail achieved by software with the minimum and maximum time required to implement the chip.

# Timing Summary for image chip

Speed Grade: -4

Minimum period: 2.414ns

Maximum frequency: 414.250MHz)

Minimum input arrival time before clock: 5.629ns

Maximum output required time after clock: 6.604ns



# 5. CONCLUSION

The design IC's for 2D and 3D image enhancement chip that leads the low power and optimized design is done in VHDL programming environment. In contrast the development is done to make programmable image chip to increase the efficiency, lower the power requirement, and reduce the delay with the comparison of previous work. Such chips can be used in digital cameras, digital oscilloscope etc. VHDL has been used to write all the programs for the IC's because of its user-friendly nature and thus modifications if required for further development shall not prove to be an obstacle. Thus the research focuses on simulation prior to fabrication. Burning these programs on FPGA (Field Programmable Gate Array) will help us to see the functional design of ICs. These results in addition to the systematic view generated would help us to design Application Specific ASIC. This work is a significant effort towards total digitization of image processing and would surely prove a boon for VLSI design industry.

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