8T sub threshold Single Ended SRAM Cell for Low Power VLSI Applications

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Abstract- At the present time data storage is gaining more prominence in human life. All electronic and digital devices prerequisite memory for decreasing the power consumption. The thought of "more data in less space" is useful for swelling the system performance and overall system competence. Generally we used semiconductor memory as "SRAM". SRAM can be truncated "Static Random Access Memory". In recent days, Static Random Access Memory has developed the major part in digital world. Because which inhabits the largest portion of SOC (system-on-chip). The device need SRAM memory mainly for device disperse small amount of power. Many VLSI chip can have SRAM memory because of their big storage capacity and fast retrieving time. Where, the word static specifies that it does not necessity to be customarily refreshed. Access Memory: (RAM). In this work the power investigation of 8 transistors SRAM is done. As a result the power dissipation and some more parameters are intended of 8 transistors and compared with 7T SRAM. Parameters are calculated and designed using DSCH software and the layouts are strained using MICROWIND software.

Keywords: 8T SRAM, Power Dissipation, Area.

1. INTRODUCTION

In modern days, Static Random Access Memory has become the main part in digital domain. Because which conquers the largest percentage of SOC (system-on-chip). The device need SRAM memory mostly for device disperse small amount of power. But the dynamic power dissipation reasons problems in digital circuits as the dynamic power areconditional on supply voltage, switching frequency and output voltage swing. Dynamic power dissipation can be reduced by dropping the supply voltage. At the same time low supply voltage hints to performance deprivation and also drops the threshold voltage which in turn raises the sub threshold current later the static power dissipation growths. This paper discuss about the power dissipation of 6 transistors and 7 transistors SRAM. It also comprises the functional opinion of 7T and 8T SRAM cells. SRAM is mostly used for the cache memory in Microprocessors, processer computers, engineering workstations and memory in hand held devices due to High speed and low power consumption. The necessity for low-power design is becoming a main issue in high-performance digital systems such as microprocessors [1], Digital Signal Processors (DSPs) and additional applications. The cumulative Market of mobile devices and battery powered portable electronic systems is generating demands for chips that intake the smallest possible quantity of power. SRAM contain of nearly 60% of Very Large Scale Integrated (VLSI) circuits. It is also supposed that memories are the biggest offender for the power dissipation in any digital system and No digital system grows complete deprived of memories. Numerous techniques have been planned to diminish the power consumption all through Write operation of SRAM like, Segmented Virtual Ground Architecture for Low-Power Embedded SRAM [2], Low power SRAM design using half-swing pulse mode methods [3] and A single-bit line cross-point cell activation (SCPA) architecture for ultra-low power SRAM's[4].Some other methods which are used for low power SRAM like Half-Swing Pulse-Mode Techniques[5] these methods are used for decrease the power dissipation of the SRAM circuit. All these deliberated papers are used extra circuitry for dropping the power consumption. In this paper augmented SRAM cell comprises two extra tail transistors in the pull-down path of the separate inverter to evade charging of the bit-lines. These two trail transistor are precise by an extra signal write select (WS). Through read or write mode at least one of the tail transistor must be twisted OFF to separate the driving path of respective inverters.

2. SRAM

SRAM or Static random Access memory is a procedure of semiconductor memory widely used in electronics, microprocessor and general computing solicitations. These form of semiconductor memory improvements its name from the fact that data is held in there in a static fashion, and does not need to be dynamically efficient as in the case of DRAM memory. While the data in the SRAM memory does not necessity to be refreshed dynamically, it is still volatile, meaning that when the power is detached from the memory device, the data is not held, and will withdraw. There are two crucial features to SRAM - Static random Access Memory, and these set it out in contradiction of other types of memory that are available: The data is detained statically: This means that the data is held in the semiconductor memory deprived of the need to be relaxed as long as the power is practical to the memory. SRAM is a form of random access memory: A random access memory is one in which the positions in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was retrieved. Fig 1 demonstrated the read/write operations of an SRAM. To select a cell, the two access transistors obligationto be “on” so the elementary cell (the flip-flop) can be associated to the interior SRAM circuitry.

3. 6T STATIC RANDOM ACCESS MEMORY

Anorthodox 6T SRAM consists 6 transistors which custom two cross coupled inverters. This bit cell can be read and write solo bit data. When a bit is stored in memory the 6T SRAM perform like a latch. The cross coupled inverter outline which causes large area consumption which is a drawback of 6T SRAM when associated to resistive load. Conventional SRAM with 6 transistors is shown in figure 1 and 6T SRAM have three states they are read, write and hold states.

3.1 Hold State

Once write operation (WL=0) the available transistor M1 and M2 disconnect the cell as of bit lines. The leakagecurrent can be haggard from vdd.

3.2. Read State

The reachable transistor M3 and M6 should be ON when pre-charging bit and bit bar line to high.

3.2 Write state

When the WL=0, the worth to be written to the bit and bit bar line. Hence we write a data value is “0”, we gross bitvalue is “0” and bit bar value is “1”.and the data value is “1”, we take bit value should be “1” and the bit bar cost is“0”.

4. 7T STATIC RANDOM ACCESS MEMORY

As peridentical 6T SRAM, the 7T SRAM circuit also contains of two CMOS cross coupled to each other. In this circuit wemoreover connect NMOS transistor to write line. And it also has two pass NMOS transistor connected to the bit and bit bar line. The contact transistor N3 and N4 which are congruently connected to the write and read line toachieve the write and read operation. Before write operation the 7T SRAM cell is contingent upon feedback connection.These feedback connection and disconnection can be achieved by N5 transistor.

4.1 Write Operation

The write operation can be flinch by rotating off the N5 transistor to this cut off feedback connection. When N3 is onand N4 is off the bit line bar transmits complement of input data. The N5 is bowed on and WL is turned off for rewire the feedback connection to stock new data. The bit line bar is satisfied to “0” for storing “1” in the cell. And there is no necessity to discharge bit line for storing “0” in the cell.

4.2 Read Operation

When accomplishment of the read operation together read and word lines are turned to on and also the transistor N5 areretained on.

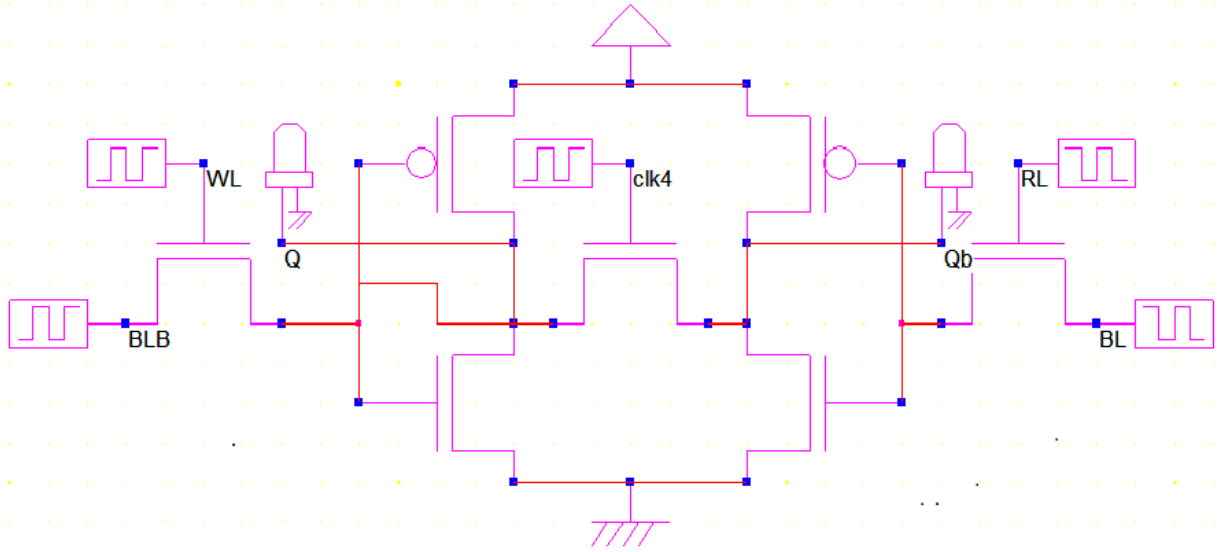


Fig.1 7T SRAM Design

5. 8T STATIC RANDOM ACCESS MEMORY

To create a cell stable in all processes, single-ended with dynamic feedback control (SE-DFC) cell is accessible in Fig. 1(a). The single-ended design is recycled to decrease the differential switching power during read–write operation. The power expended during switching/toggling of data on single bit line is lesser than that on differential bit-line pair. The SE-DFC allows writing complete single nMOS in 8T. It also splits the read and write path and displays read decoupling. The structural change of cell is measured to improve the immunity against the process–voltage–temperature (PVT) variations. It improves the static noise margin (SNM) of 8T cell in subthreshold/near-threshold area. The proposed 8T has one crosscoupled inverter pair, in which each inverter is completed up of three cascaded transistors. These two stacked cross-coupled inverters: M1–M2–M4 and M8–M6–M5 clamp the data during hold mode. The write word line (WWL) controls only one nMOS transistor M7, recycled to transfer the data from single write bit line (WBL). A separate read bit line (RBL) is used to transfer the data from cell to the output when read word line (RWL) is triggered. Two columns prejudiced feedback control signals: FCS1 and FCS2 lines are used to switch the feedback cutting transistors: M6 and M2, respectively.

In order to progress the performance of conventional SRAM cell during normal mode (Read and Write) and standby mode (SRAM contains previously written value) with the decrease in power consumption and leakage current there is one method to make alteration in conventional SRAM circuit in such a way that the proposed SRAM circuit help in falling the power consumption and leakage current and also accomplishes the charging and discharging the bit line during read and write operation. .

In this new SRAM cell the read operation and write operation is achieved by two different word lines WWL and RWL. During write operation RWL is low and WWL is triggered similarly during read operation the WWL is low and RWL is high. There is one another transistor is connected between the two cross coupled inverters that will help in dropping the effective resistance of the pull down network of inverters and is liable for read operation by connected the gate of this transistor to the RWL (read word line) signal. Last one transistor also additional in new proposed SRAM cell nearly one of the contact transistor to create a distinct path for read operation of new SRAM cell by connecting RWL signal with gate of this transistor and drain incurable is connected at output of one inverter. The schematic circuit of planned SRAM is shown in figure (2)

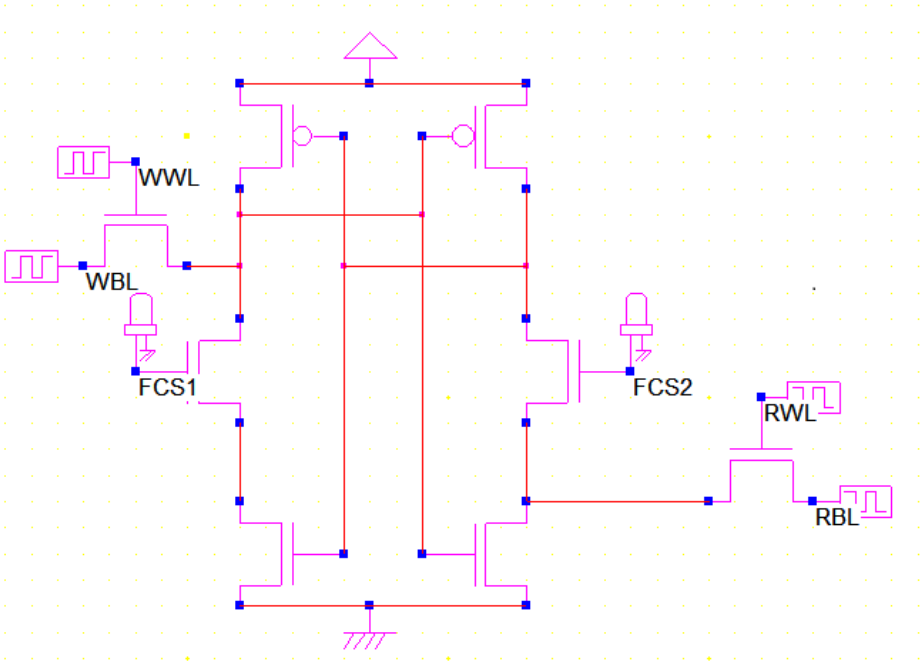


Fig.2 8T SRAM Cell Design

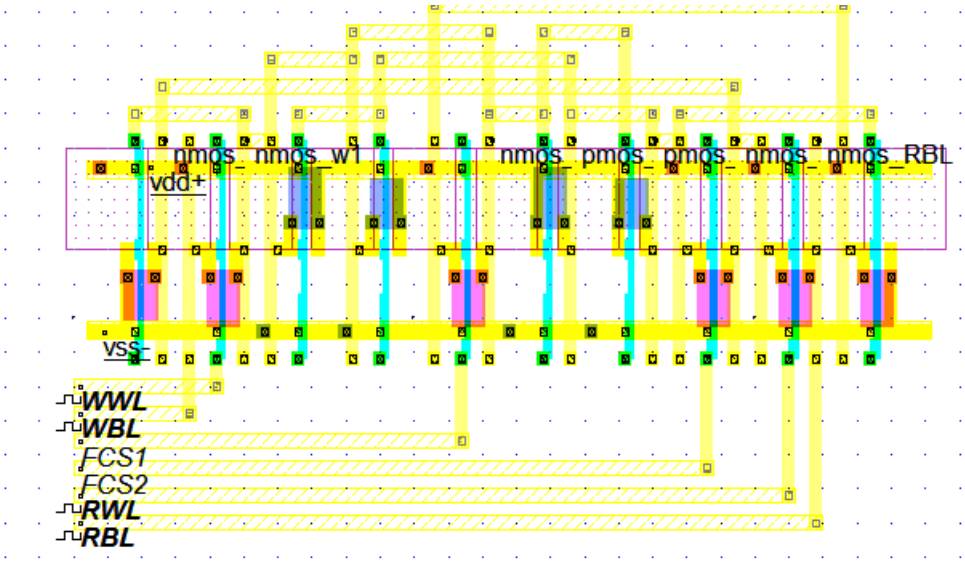


Fig.3. Layout of 8T SRAM cell with single ended

Verilog | Hierarchy | Netlist | Critical path

Symbol n°	Name	Pins	Nodes	Model	Regs	Misc.
1	nmos	s,g,d	0,2,3	901	- - 16	0.000
2	nmos	s,g,d	4,5,2	901	- - 30	0.000
3	pmos	s,g,d	2,6,1	902	- - 16	0.000
4	nmos	s,g,d	7,8,2	901	- - 30	0.000
5	pmos	s,g,d	1,2,6	902	- - 23	0.000
6	nmos	s,g,d	6,9,3	901	- - 16	0.000
7	nmos	s,g,d	3,10,11	901	- - 9	0.000
8	nmos	s,g,d	7,6,0	901	- - 16	0.000
9	vss	vss	0	0	-	0.000
10	clock1	WWL	5	69	0	0.000
11	clock2	WBL	4	69	0	0.000
12	vdd	vdd	1	1	-	0.000
13	light4	FCS2	9	49	-	0.000
14	clock3	RWL	10	69	0	0.000
15	light2	FCS1	8	49	-	0.000
16	clock4	RBL	11	69	0	0.000

Fig .4.Net List generation of 8T SRAM cell

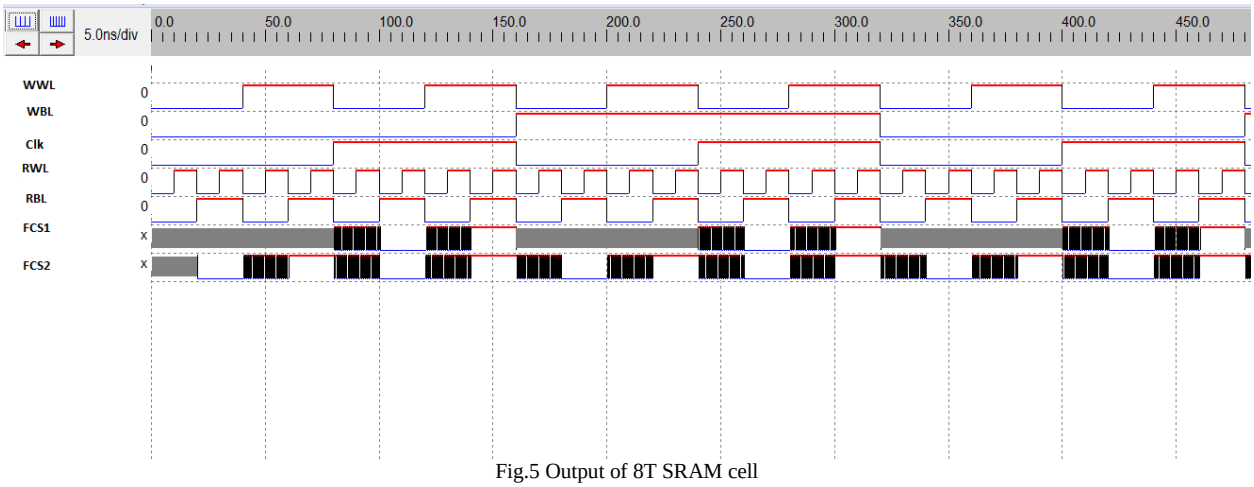


Fig.5 Output of 8T SRAM cell

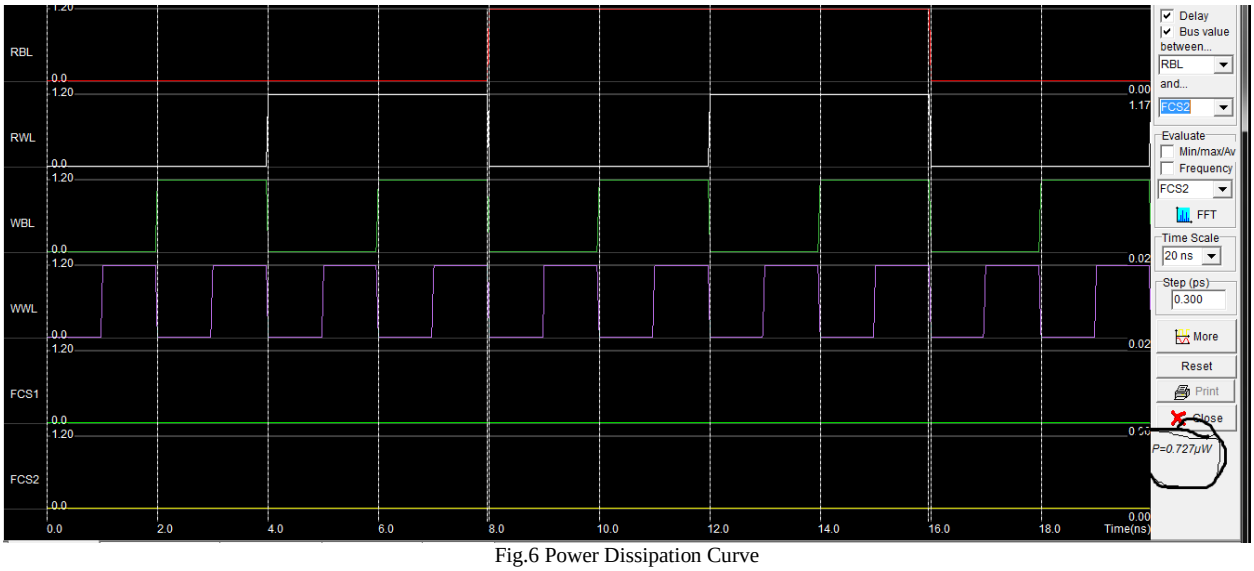


Fig.6 Power Dissipation Curve

The fig. 6 demonstrations the power dissipiation characteristics of the SRAM. Fig. 7 and 8 shows the association between Ids vs. Vds and Ids vs. Vgs respectively. Yielding to the DC characteristic it can be coherent that theMOS is not biased from its normal operation and the subthreshold effect is also negligible so the low power operation is obligatory.

Fig.7.Drain Current Vs Gate Voltage Curve

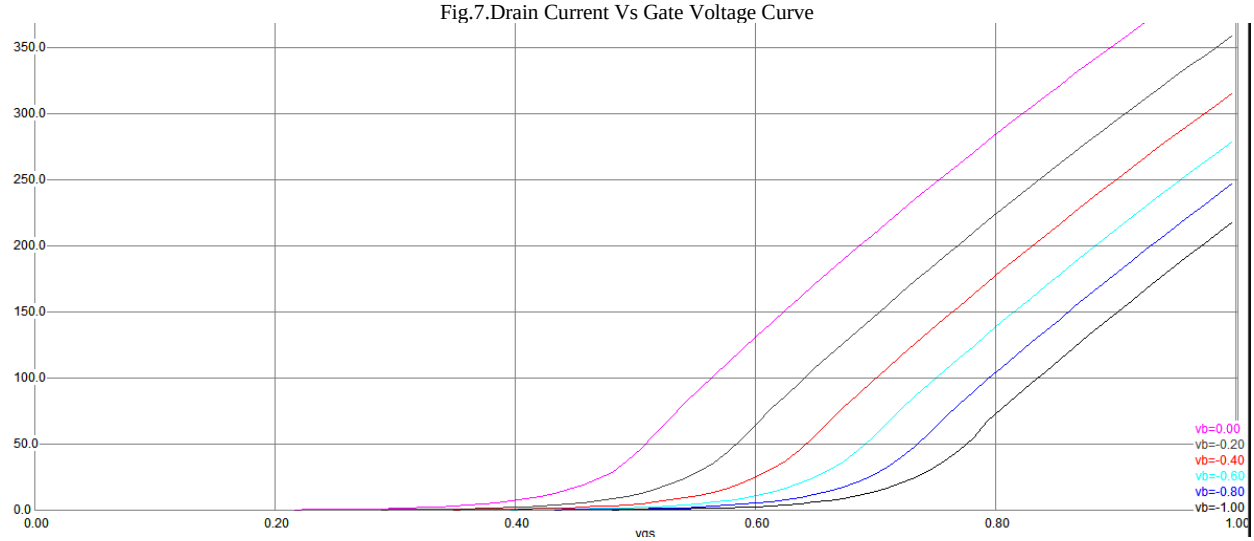


Fig.8. Drain Current Vs Drain Voltage

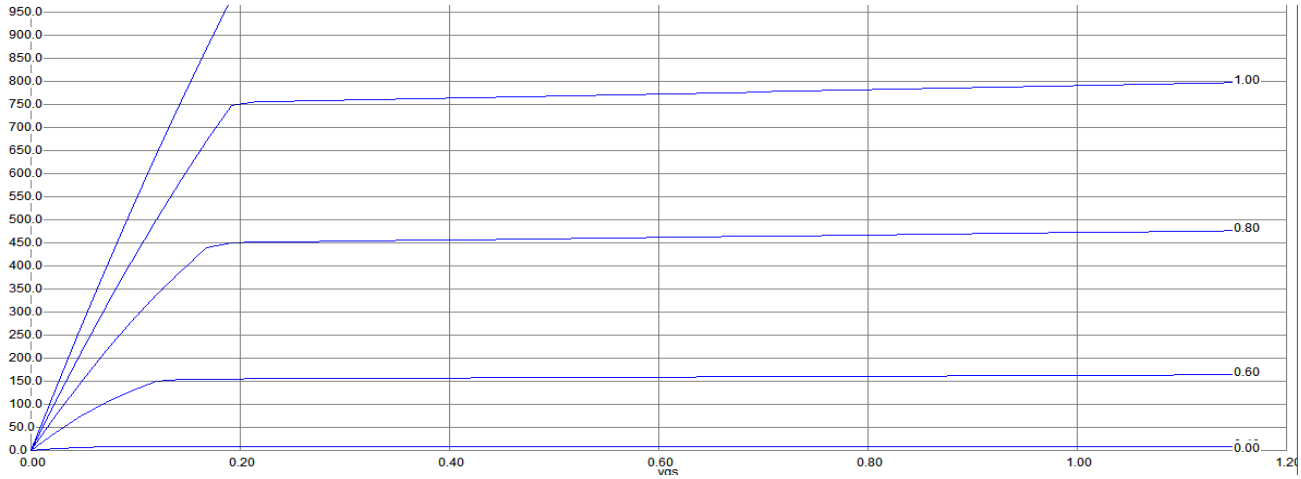
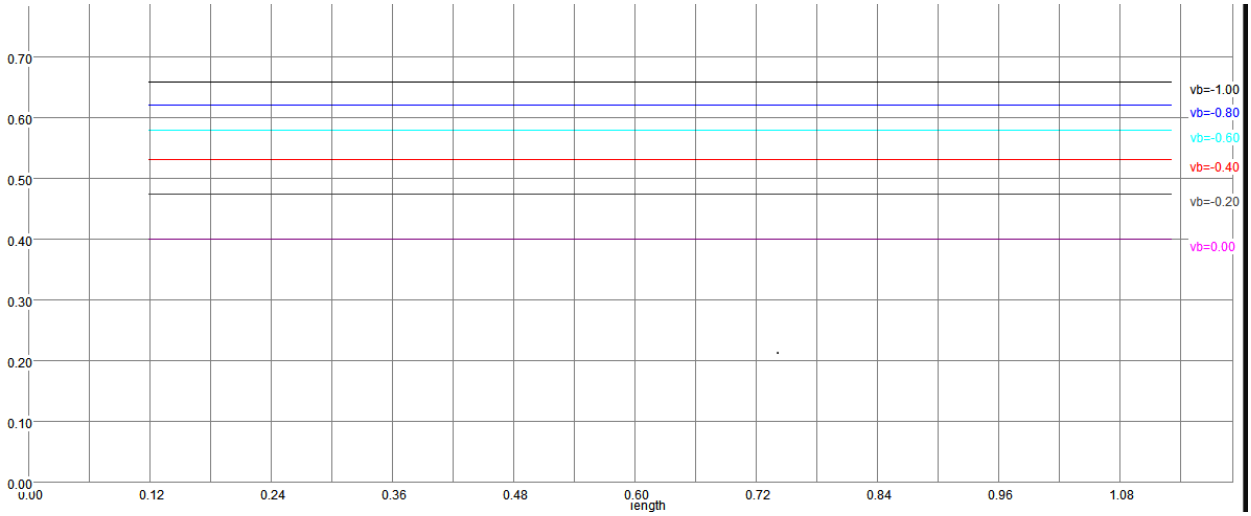


Fig.9 shows the relationship between channel length and the threshold voltage, laterconvinced limit is turned ended for short channel the threshold roll off is well strong-minded from the graph which will help in the determining the proper channel length of the device and it recovers the, device operation. Capacitances are augmented in such a fashion that it will not disturb the circuit performance. The final optimized simulation assessment is shown in figure – 10.

Fig.9.Threshold Voltage



CONCLUSION

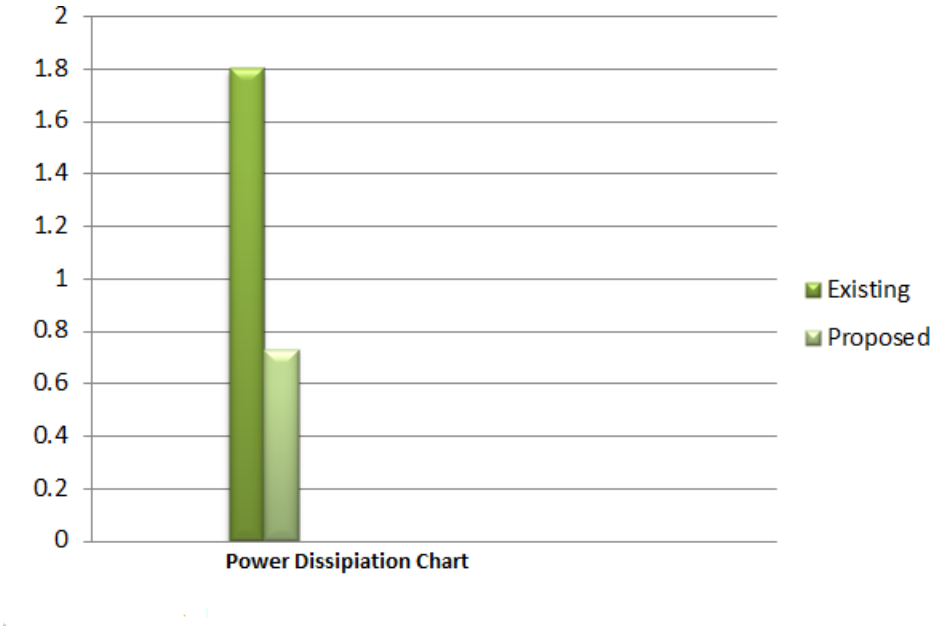


Fig.10. Simulation comparison of SRAM cells

In this paper power dissipation of 8T SRAM is associated with 7T SRAM. Simulation and analysis of 8T SRAM and7T SRAM is anticipated. Simulation result demonstrations clearly how read and write operation is executed. It is pragmatic that the power dissipation is less as compared with 8T SRAM to the 7T SRAM in read as well as write mode of operation. In future, power dissipation will show a major role to compact power consumption.

ACKNOWLEDGEMENT

This work was supported in part by the Baba Institute of Technology, Visakhapatanam.

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