Realisation of QCA Based Adder Circuit for High Speed Application

K. Santhu Sravani
M.Tech Scholar, Department of ECE
Baba Institute of Technology and Sciences, Visakhapatnam
sravani0125@gmail.com

Mrs. BVR Gowri
Assistant Professor, Department of ECE
Baba Institute of Technology and Sciences, Visakhapatnam
gowri.bobbili@bitsvizag.com

B. Siva Prasad
Associate Professor, Department of ECE
Baba Institute of Technology and Sciences, Visakhapatnam
hodece@bitsvizag.com

Abstract- In the existing technologies, Quantum-dot Cellular Automata (QCA) is recently proposed alternative method in the CMOS design. It is one of the best method to design high speed digital and ultralow-power circuits. Several binary and arithmetic circuits are implementing using QCA technologies, but still some improvements are possible if the logic gates are constitutionally accessible in these technologies.

This short proposes a new procedure to design QCA-based BCD adders. In this paper ripple carry adder using majority gates as a existed system and brunt kung adder using majority gate as a proposed system. Utilizing new logic assembling and purpose-designed QCA modules, area and consumption of power significantly lower than existing system.

Key Words—Quantum-dot Cellular Automata (QCA), BCD adders, decimal arithmetic.

1. INTRODUCTION

QCA technology has become one of the most attractive approaches for the development of next-generation ultra dense low-power high-performance digital circuits. Among the logic circuits recently proposed, arithmetic sub modules represent examples of the most investigated structures. Independently of the performed logic function, the modules are designed smartly combining inverters and majority gates (MGs), these are the only fundamental logic gates available within the QCA technology. Decimal arithmetic has recently a great deal of attention since several financial, commercial, and Internet based applications increasingly require higher precision.

This brief proposes a new approach to design QCA-based technologies n-digit (with $n \geq 1$) BCD parallel adders are able to achieve increasing speed higher than present counterparts without sacrificing

either the occupied area or the cell count. The main advantages are increasing computational speed, decreasing area are obtained by exploiting a new novel logic designed QCA modules.

The latter have been optimized by taking into account that the most time critical decimal addition between two *n*-digit numbers occurs. It must adding of least significant digits. It will be carry generated of the operands. It is then propagation of subsequent bits positioning and finally some digits are computated by using of MSB.

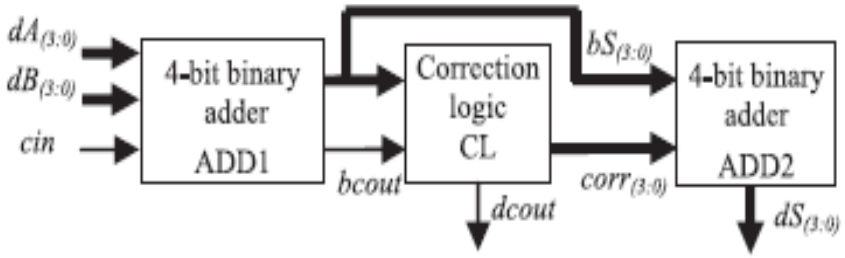

Fig1. Structure of the BCD adders .

(a)QCA Cells

The cells are processing an two stable orientation state which has quadra-pole electric state by that two stable orientation state which has happened represents the two binary bits like “0” and “1” of QCA cell structure. In QCA cell structure consisting of two quantum dots arranged in particular square manner. In this processing of QCA cell based on the columbic interactions between many identical QCA cells.

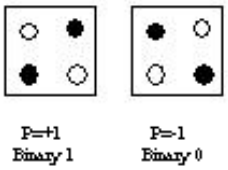

Fig2: Basic QCA cell and Two Possible Polarizations.

In this QCA cells containing of 4 dots like two electrons and two holes which is ripples to each other as well as result of mutual combinations. In that columbic interaction and ground state technology to occupy the diagonal dots of the cell.

In this two polarization the QCA cell denoted P=+1 & -1 respectively. If P=+1 binary logic is “1” as well as P=-1 binary logic is “0” encoded in polarization. If a cell placed on near the cell by using columbic interaction removing of divergence and determines ground state of the first cell propagation of second cell.

(b)QCA Wires

In that QCA wires a cells of binary signal that can be communicated another cell its going on the from input to output because of the electrostatic interactions between cells. This performing of operation

each and every clock cycle should be half of the wire is active for signal propagation when ever be half of the wire is unpolarised.

When ever the device is operating the next clock cycle should be half of the previous active clock zone is disabled and remaining wire is to be in activated zone triggering the input cells to be polarised. Then propagation of signals from one clock to another clock zone.

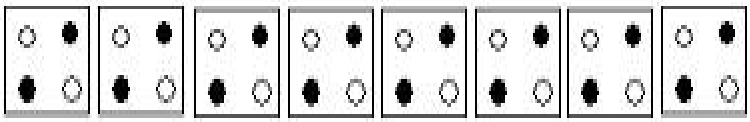

Fig3: QCA Wires

(c)QCA gates

These gates are implemented by full adder carry expression and it acts as basic gates of QCA.

M (A, B,C)=AB+BC+AC

QCA gates are implemented with And OR logic gates from making 3 input majority gate.

M (A, B, 1) =A+B

M (A, B, 0) =AB

Fig4: QCA Majority Voter Gate

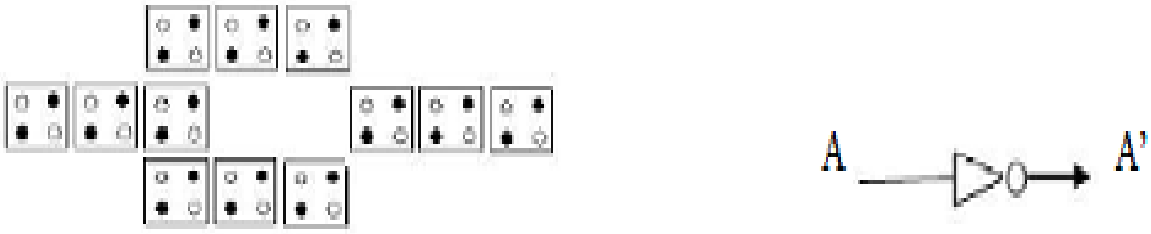

Fig5: QCA Inverter Gate

In QCA we were discussed the functionality in the last chapters. In this chapter the simulation and synthesis results of the Binary Adder in terms of Sum and Carry Chain. Here Xilinx 14.7i tool is used to synthesis and simulate the design and verification of functionality od design. Once the functional verification is done, the design will be taken to the synthesis and simulation of Xilinx tool for process and the net list file generation.

In order to find synthesis and simulation results of appropriate test cases have been identified in order to test this modeled QCA design. Depends on the identified values, the simulation results describes the operation of the QCA Adder has been achieved. This model proves the works properly as per the process.

2. RIPPLE CARRY ADDER IN QCA TECHNOLOGY

To introduce the RCA architecture in this existed system parallel adders in QCA are implementing, let consider two *n*-bit address $A = an-1,. . . , a0$ and $B = bn-1, . . . , b0$. Let us take i^{th} bit position (with i = n-1,.....,0). In this process two signals are obtained namely propagation and generation signals.

Propagation signal pi=ai+bi and

Generation signal gi=ai . bi

The computed signal initially cin can be produces the carry at the i-1 bit position the carry signal ci+2, furnished at the $(i+1)^{th}$ bit positions can be implemented using the conventional CLA logic represented as below after it can be rewritten as given in equation, by exploiting Theorem.

In general the propagation of carry in RCA through the subsequent bit positions, but it requires only one MG. In this MG circuit operating in the RCA process. The two cascaded MG's to perform the addition operation between RCA and CFA. In our project RCA adder designed as existed has worst case path to overcome with respect to the brent kung adder.

Equation is exploited in the design of the novel 2-bitmodule shown in Fig. 1 that also shows the computation of the carry $ci+1 = M(pi\ gici\ )$. The existed *n*-bit adder is then implemented by cascading *n*/2 2-bit modules as shown in Fig. 6(a).

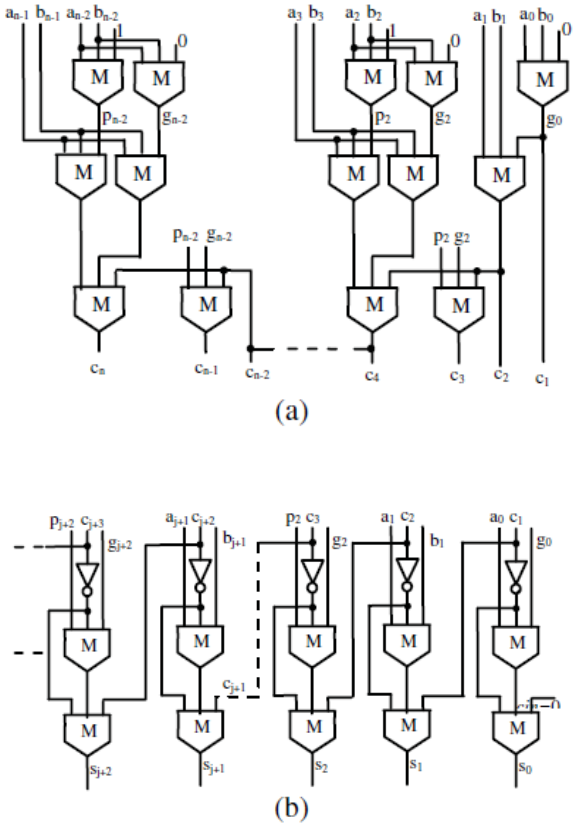

Fig 6: RCA *n*-bit adder (a) carry chain and (b) sum block

Suppose if we have assumed that the carry-in of the adder is *cin* = 0, the signal *p*0 is not required and the 2-bit module used at the least significant bit position is simplified.

The sum bits are finally computed as shown in Fig. 6(b). In this process the performing of addition in complexity. When generated carry at least significant bit g0=1 as well as propagated through the consequent bit positions at the MSB side. In this the first two bit modules was computes worst case of computational path with two cascaded MG's by contributing of C2.

The module is cascading of MG is equal to (n-2)/2 with only one MG. By considering remaining two MG's one MG is required to invert and compute the sum. The worst case of RCA consisting of following equations.

$ci+2 = gi+1 + pi+1 \cdot gi + pi+1 \cdot pi \cdot ci$ -------(1)

$ci+2 = M(M(ai+1, bi+1, gi)\ M(ai+1, bi+1, pi)\ ci)$---------(2)

3. BRENT KUNG ADDER

These adders are used to perform binary additions. In order to get parallel prefix adder CLA structure was used. The algorithm is the tree structure to increase speed of operation. These adders are highly used in industries to increase speed of operation.

The construction of parallel prefix Adder involves three stages:

1. Pre-possessing stage:- Generate and propagate signals to each pair of the inputs A and B are computed in this stage.

Propagation (Pi) and generation (Gi) were represented in QCA technology

Pi = Ai xor Bi

$=Ai.\overline{B} + Ai.Bi$

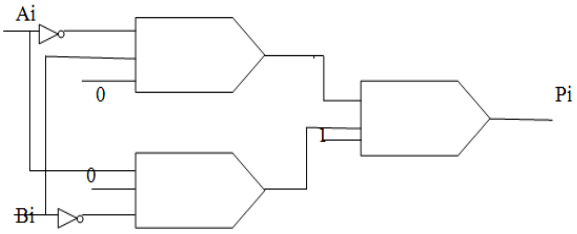

Fig 7: Propagation circuit

Gi = Ai and Bi

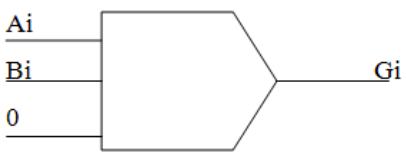

Fig 8: Generation circuit

2. Carry generation network:- In this stage, carries equivalent to each bit is calculated. All these operations are implemented and carried out in parallel.

CPi:j = Pi:k+l and Pk:j

CGi:j = Gi:k+l or (Pi:k+l and Gk:j)

CP0 = Pi and Pj

CG0 = (Pi and Gj) or Gi

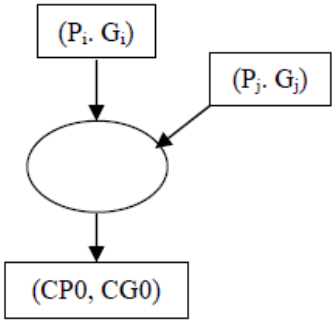

Fig 9: Carry network

CP0 and CG0 were represented in majority gates

Carry propagation CP0 = Pi and Pj

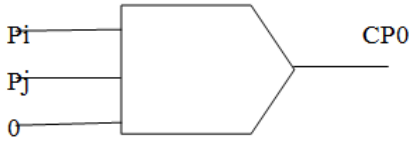

Fig 10: circuit diagram for carry propagation

Carry generation CG0 = (Pi and Gj) or Gi

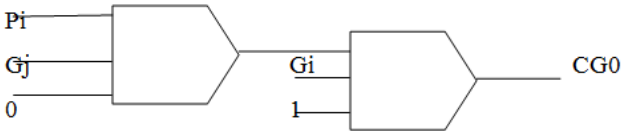

Fig 11: circuit diagram for carry generation

3. Carry Network Post processing Stage:- This is the concluding step to compute the summation of input bits.

Ci-1= (Pi and Cin)

Si =Pi xor Ci-1

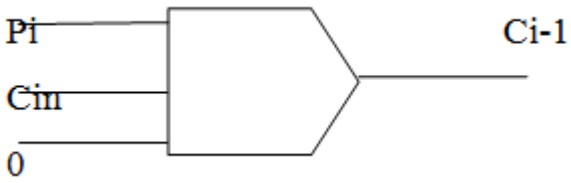

Fig 12: Final carry Generation

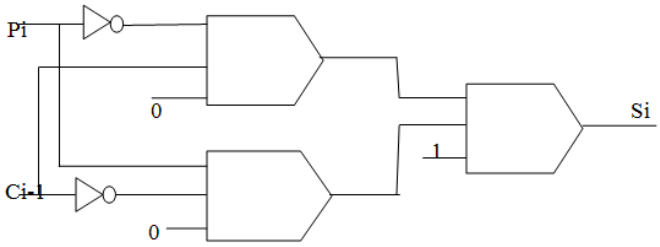

Fig 13: Final sum generation

Brent-Kung adders are widely used. It gives good number of stages of inputs to outputs. It is parallel prefix adder where intermediate stages were used.

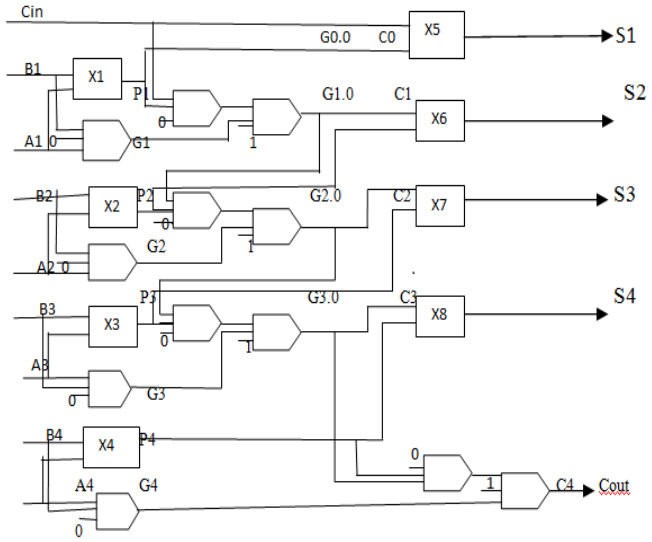

Fig 15: bit brunt kung adder using majority gates

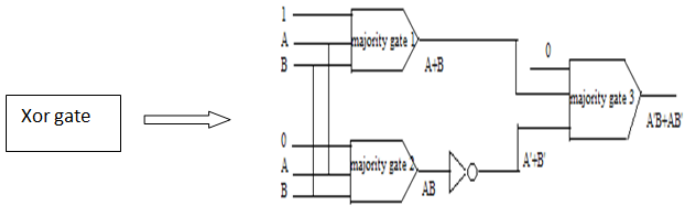

Fig 16: xor gate using majority gate

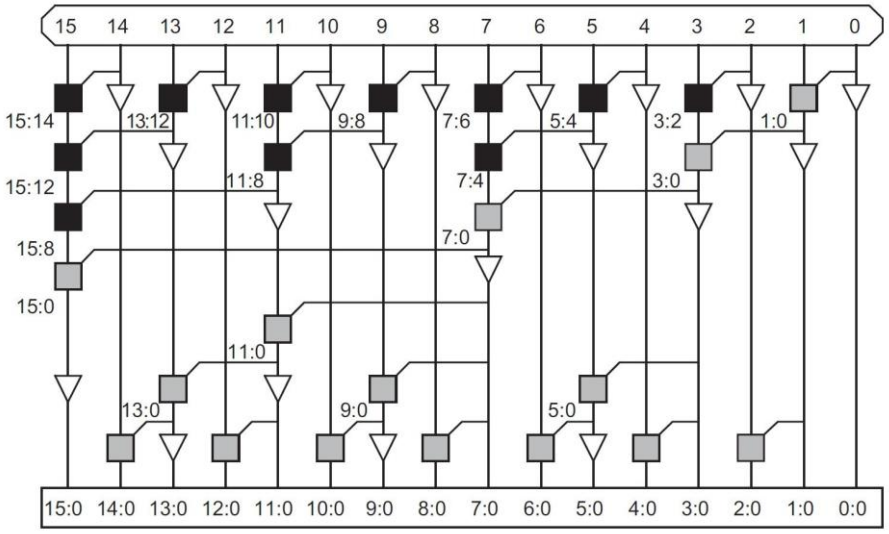

Fig 17: 16-bit Brent Kung Adder

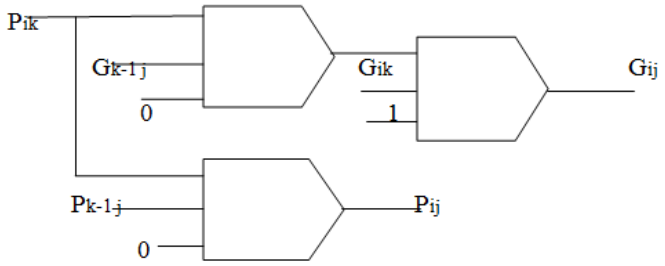

Fig18: black cell by using majority gates

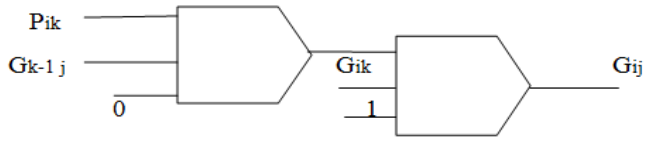

Fig19: Gray cell by using by using majority gates

4. RESULTS

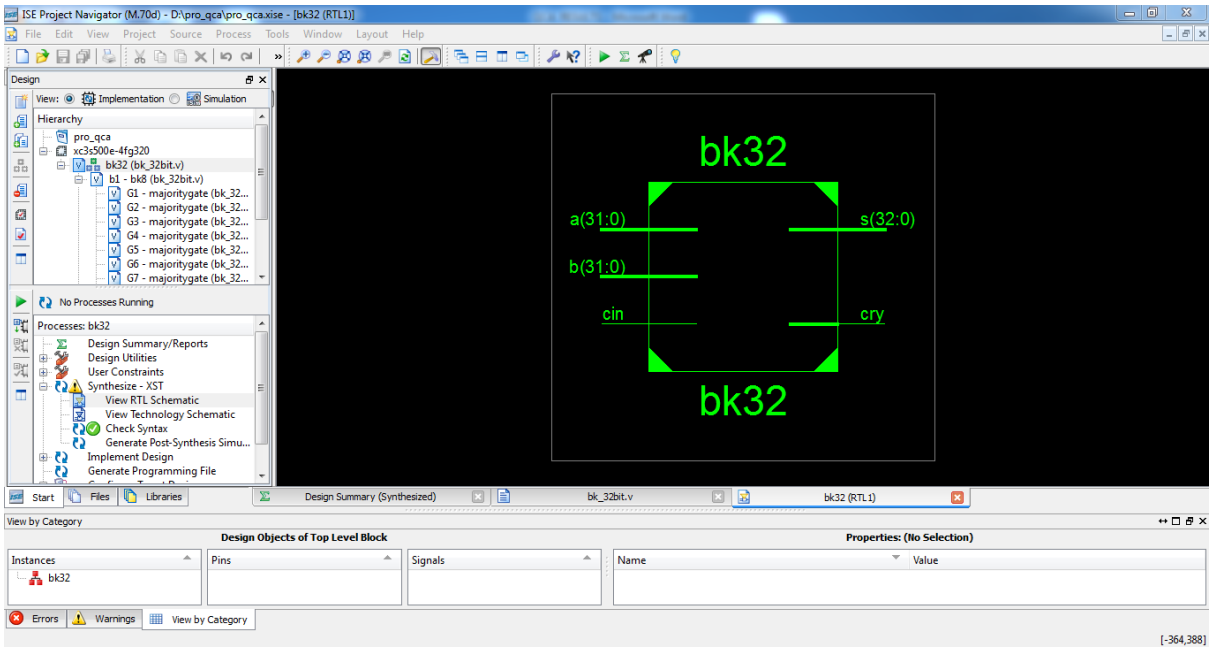

Fig: RTL Schematic view

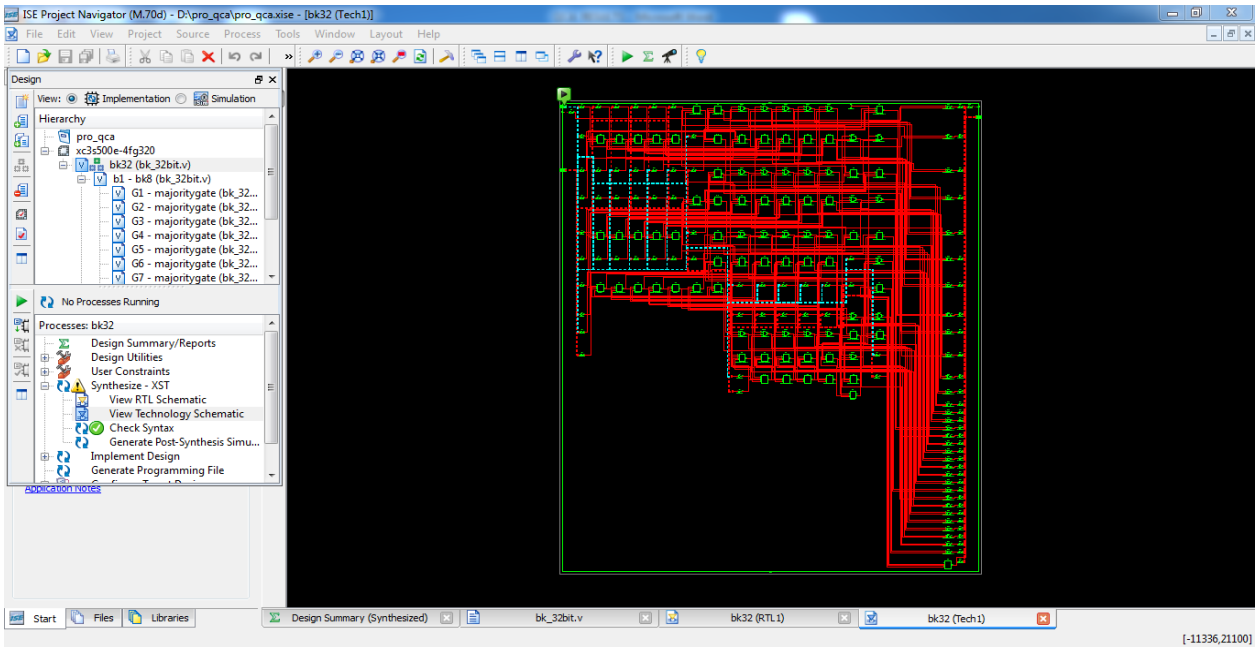

Fig: View Technology Schematic

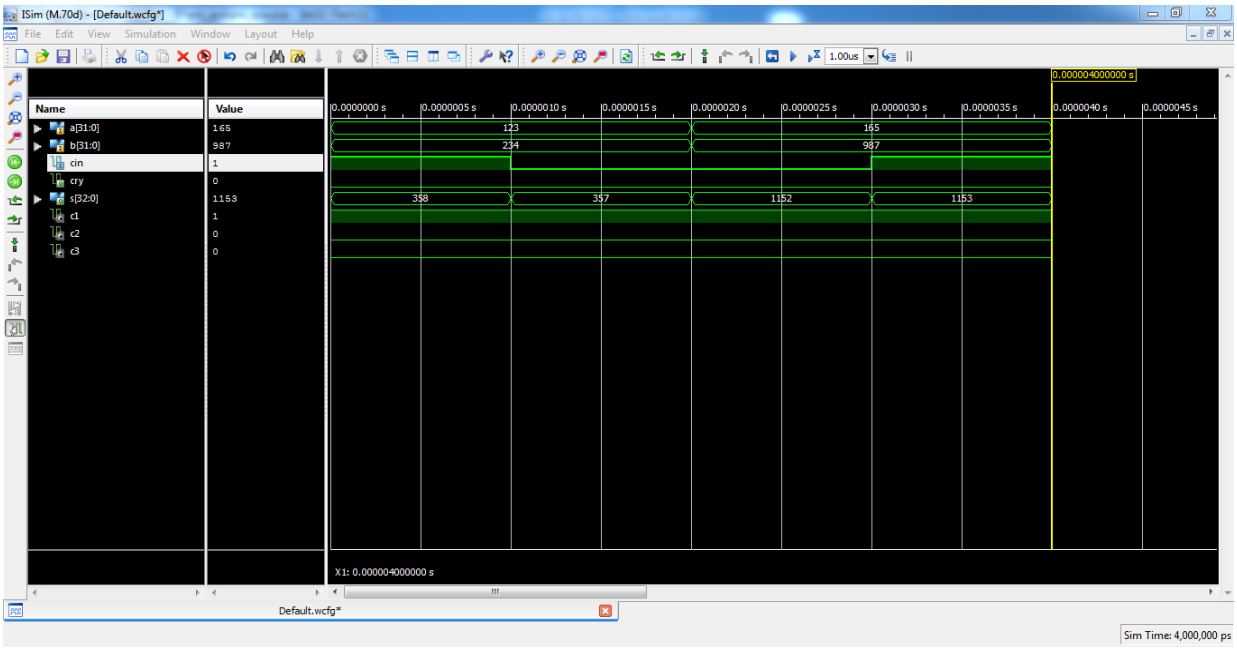

Fig: Simulation results for QCA

Adder	No of LUT 'S	Delay	Power
Existing system	76	15.210ns	0.6196mw
Proposed system	60	16.679ns	0.4892mw

Table: comparison table

5. CONCLUSION

In this paper, it was introduced BRENT KUNG ADDER using majority gates in QCA technology was proposed system, and using majority gates in RIPPLE CARRY ADDER was the existed system. The proposed brent kung adder gave best results compared to the existed ripple carry adder. In addition the brent kung adder occupies less power and low area compared to the majority gate in RCA. The proposed method brent kung adder structure is better than the remaining parallel adders for the application of both the area and power consumptions are critical.

REFERENCES

[1] V. Pudi and K. Sridharan, "Low complexity design of ripple carry andBrent–Kung adders in QCA," *IEEE Trans. Nanotechnol.*, vol. 11, no. 1,pp. 105–119, Jan. 2012.

[2] K. Sridharan,and V. Pudi "Efficient design of a hybrid adder in quantumdot cellular automata," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*,vol. 19, no. 9, pp. 1535–1548, Sep. 2011.

[3] S. Perri and P. Corsonello, "New methodology for the design of efficientbinary addition in QCA," *IEEE Trans. Nanotechnol.*, vol. 11, no. 6,pp. 1192–1200, Nov. 2012.

[4] V. Pudi and K. Sridharan, "New decomposition theorems on majoritylogic for low-delay adder designs in quantum dot cellular automata,"*IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 10, pp. 678–682,Oct. 2012.

[5] K. Walus and G. A. Jullien, "Design tools for an emerging SoCtechnology: Quantum-dot cellular automata," *Proc. IEEE*, vol. 94, no. 6,pp. 1225–1244, Jun. 2006.

[6] S. Bhanja, M. Ottavi, S. Pontarelli, and F. Lombardi, "QCA circuits forrobust coplanar crossing," *J. Electron. Testing, Theory Appl.*, vol. 23,no. 2, pp. 193–210, Jun. 2007.