Johnson Counter Using Master Slave D Flip Flop

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Abstract- In a digital system the contribution of Sequential circuits is very large in terms of power dissipation and propagation delay. For VLSI back end designers maintaining low power with less delay and efficient area has been the major concern in sequential circuit design. An optimized design technology is to be selected to achieve the above mentioned parameters. Counter is one of the sequential circuit which have wide applications in the area of microcontroller circuits which includes PLL, D-A converters, signal generators and synthesizers etc. In this paper a 4 bit Johnson counter is proposed, which exhibits features like low power, high speed and cost efficient. To realize the negative edge triggered master slave D flip flop, a deployed flip flop circuit is designed which uses 14 transistors. Comparative analysis in terms of performance and cost is done against the conventional counter and proposed design. It is found to be 43.22 % of lesser power dissipation in the proposed design than conventional design. When compared to conventional design the transistor requirements in the proposed counter is 69.5 % lesser which makes it an optimized design in terms of area.

Keywords - Johnson Counter; Master Slave D flip flop; VLSI; Power Dissipation, Area.

I. INTRODUCTION

Counters play an important part in digital systems which were required to generate sequences synchronously in different forms. A digital counter consists of flip flops set that change their states to generate particular pattern of sequence in a specific manner. This sequence pattern could be associated with controlling a digital system or number of times an event occurs. Counter is one among the sequential circuit which have applications in wide range, the area of microcontroller circuits which includes signal generators and synthesizers , PLL, D-A converters, etc, frequency synthesizers, digital timing, digital memories and dock circuits etc. The output patterns of 0's and 1's are referred to as its states that are stored in various flip flops of counters. The total number of states in a counter is called its modulus count and the manner in which a counter passes through these states is referred to as its counting sequence. Sequential circuits are integrated along with combinational circuits in small area of a chip, in VLSI designing. Sequential digital circuits including registers and counters are used to perform all memory processes, arithmetic and logical operations in a computer system. So for the best performance of the computer systems these sequential circuits must be designed effectively and efficiently. Low power and area efficient design are key goals for a developer. Adopting proper architecture can lead to

designing of a low power circuit with minimum number of CMOS logic gates. The selection of design technology and flip flops used play key role in power reduction.

Johnson counter is one of very useful counters in computer design which generates a specific data pattern in synchronous manner. This data pattern is used in various logic designs to implement desired logic functions. Conventional model Johnson counter is designed by using shift registers, as all of the flip-flops were provided with clock of same pulse for synchronous operation. Conventional D flip flops are generally made up of NAND gates and inverter. In Johnson counter design the inverted output of the LSB flip-flop is connected to input of the MSB flip-flop. All other flip flops derive their inputs from the output of next higher significant flip-flop bit.

In the Johnson counter that was proposed Master-Slave D flip-flops are used with minimum number transistors, in the place of conventional type master slave D flip-flops, as it reduces the transistor count, the speed of the design also enhanced. Low transistor design in turn reduces the power dissipation in the circuit. The proposed Johnson counter is designed using Tanner tools. The contribution and outline of this paper is as follows:

Section II describes the design considerations of the CMOS circuit implementation. Section III presents the design of Johnson counter circuit. Section IV provides the details of the proposed schematic design. Section V gives the discussion on the simulations and results which were obtained from the schematic of 4 bit Johnson counter in Tanner EDA and finally section VI concludes the paper.

II. DESIGN CONSIDERATIONS

One of the design goals in VLSI has been to reduce the power consumption in CMOS logic circuits. In various applications, power consumption in CMOS logic designs has increased due to the use of continuously increased dock frequency. Even when used at lower supply voltages these designs exhibit higher power dissipation. Power consumption in CMOS logic circuits consists of a static component resulting from leakage of inactive devices, gate tunnelling current, threshold conduction through inactive transistors, contention current etc. [4]. The sub-threshold current can be expressed as:

$$I_{ds} = I_{dso} e^{\frac{V_{gs}-V_t}{nV_T}} \left(1 - e^{-\frac{V_{ds}}{V_T}}\right)$$

$$\text{Where } I_{dso} = \mu_{eff} . c_{ox} . \left(\frac{W}{L}\right) . V_T^2$$

J_{ieff} refers to the effective charge carrier mobility,

Cox is gate capacitance per unit area, L is width to length ratio of the channel, V_t represents threshold voltage, V_T is thermal voltage, n refers to sub threshold swing coefficient and V_{gs} and V_{ds} represent gate to source and drain to source voltages respectively [5]. Dynamic power dissipation arises because of charging and discharging of load capacitance and short circuit current that flows while the switching of CMOS transistor takes place. The finite nonzero load capacitance gets charged when PMOS is on and as soon as NMOS gets activated it gets itself discharged by providing current through itself to ground. The power dissipation due to charging and discharging of load capacitance is expressed as:

$$P = 0.5\, C_L\, V_{DD}^2\, f_{clk}\, E_{sw}$$

Where C_L is the load capacitance, VDD is the supply voltage, f_{clk} is the dock frequency and E_{sw} refers to the average switching activity i.e. average number of output transitions per dock cycle. Since dock frequency in high speed applications has increased, it has resulted in high switching frequency of CMOS devices resulting in higher dynamic power dissipation [6]. Sequential circuit largely contributes to the power dissipation of a digital

system. Sequential circuit changes its present state synchronously with the dock transitions according to the specified logic. These state changes can occur either during positive or negative edge transitions of dock. Clock transitions from high to low and low to high, are themselves big contributors to the power dissipation. In CMOS designing while dock transition occurs, both NMOS and PMOS can be activated for a fraction of time because of non-zero rise time and fall time. It creates an electrical path from VDD to ground and current flows through the circuit. This current is referred to as Short circuit current or thorough current which appear as a spike during dock transition [6]. This short circuit current leads to a major portion of dynamic power loss which is referred to as short circuit power dissipation and is expressed as follows:

$$P_{sc} = I_{sc}.V_{dd}.t_s.E_{sw}$$

where, I_{sc} is short circuit current and ts is the switching delay [5]. These two above described phenomena account for dynamic power dissipation in sequential circuits which heavily depend upon dock switching frequency. It has been shown that dock signals even account for 15 to 45 % of total power dissipation [7].

III. JOHNSON COUNTER DESIGN

In sequential logic circuits the basic memory element is flip flop. It can store data on rising edge or falling edge of the dock pulse. Flip flop that operates on rising edge of dock pulse is referred to as positive edge triggered flip flop and one that operated on falling edge is called negative edge triggered flip flop [2]. A conventional master slave D flip flop is designed using 8 NAND gates and an inverter as shown in Fig. 1. The first stage of master slave flip flop is called the master which is directly applied with extern al dock pulse signal and the second stage which is referred to as slave is applied with the inverted dock. The master is sensitive to the positive level of the dock while the slave to the negative level.

When extern al dock signal is at high level, master is operational and it follows the D input. Simultaneously the slave is deactivated and therefore holds its previous value. When dock transition takes place to logic 0 from logic 1, the master latch samples its output value and passes it to slave. The slave is activated for low dock signal level and hence it passes the stored value to its output. During negative level of dock the master is deactivated and hence is unaffected from the input applied to it. Here an area efficient and low power Master Slave flip flop is used which is negatively edge triggered i.e. Slave output is updated at the low dock signal level [8]. In the proposed Johnson counter a negative edge triggered master slave D flip flop with less transistor count is used. The transistor level implementation of the above mentioned flip flop is as shown in Fig. 2 [9]. It has a transistor count of 10 which is lesser than the conventional master slave D flip-flop. However, the shown master slave D flip flop cannot be used in counter circuits as there is no provision to reset it. Therefore it is further associated with 2 additional NMOS transistors which are used to reset its state. This takes the transistor count to 12 but provides much required reset operation for counter applications. The transistor count of the proposed master slave D flip flop still remains lesser than the conventional master slave D flip flop. Johnson counter, conventionally, is based on synchronous timing principle where the state of each flip flop is evaluated at every triggering edge of clock. The modulus count of Johnson counter is 2n where n is the number of flip flops used in its design. The block diagram of 4 bit Johnson counter and its count sequence are shown in Fig. 3 and Table 1 respectively. In 4 bit Johnson counter the modulus count is 8. Initially the state of the counter is reset to 0000. It

then follows the count sequence as 1000, 1100, 1110, 1111, 0111,0011, 0001 and then back to 0000. Johnson counter is also called as twisted ring counter because instead of connecting the least significant flip flop output to most significant flip flop input, as is done in ring counter, the inverted output of least significant flip flop is connected to the input of most significant input [7].

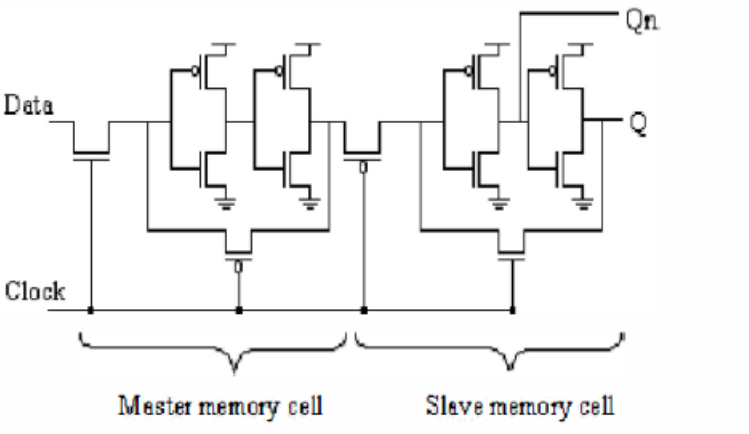

Figure 1: Negative Edge Triggered D Flip Flop

TABLE 1: STATE TABLE OF 3 BIT JOHNSON COUNTER

Clock	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

TABLE 2: NMOS AND PMOS SPECIFICATIONS

Parameter	NMOS Transistor	PMOS Transistor
Length	45 nm	45 nm
Width	120 nm	240 nm
Finger width	120 nm	240 nm
Fingers	1	1
S/D metal	400 nm	400 nm
Threshold	800 nm	800 nm

IV. PROPOSED SCHEMATIC DESIGN

The proposed circuit of Johnson counter has been simulated and implemented for 45nm technology in Cadence EDA tool. The transistor level schematic is designed in Cadence Virtuoso schematic editor [9]. The circuit is implemented progressively by creating instances of various components in the design and then putting them together to get the desired response of Johnson counter. The PMOS and NMOS transistors used to build the schematic diagram are selected as per the specifications tabled in Table 2. Using the transistors of above mentioned specifications, less transistor count master slave D flip flop is designed as shown in Fig. 4. It

employs 10 transistors to execute the performance of master slave D flip-flop. An inverter cell is created with same transistor specifications and is directly used in the schematic. 2 additional NMOS transistors are used in the circuit for reset operation. A cell of the designed flip flop is created so as to use it as an instance in the Johnson counter designing. Subsequently, the proposed 4 bit Johnson counter is designed using the instances of master slave D flip-flop. The implemented design is shown in Fig. 5 which is then simulated and analyzed using Cadence analog design environment.

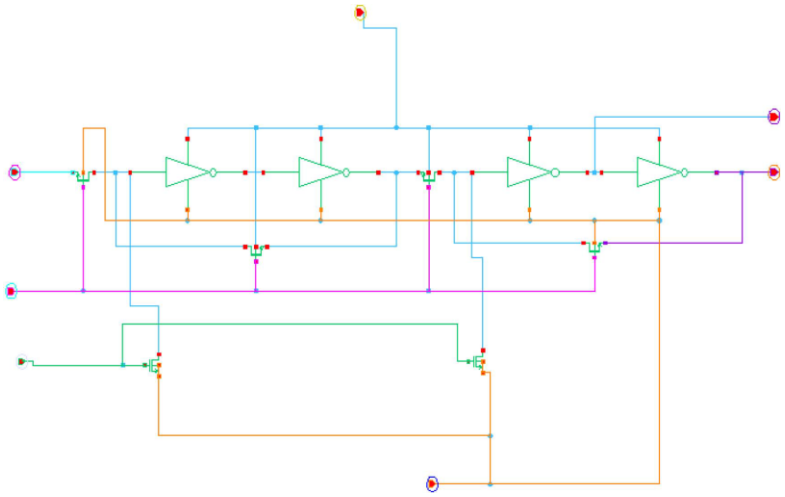

Figure 2: Master Slave D Flip Flop with less transistor count

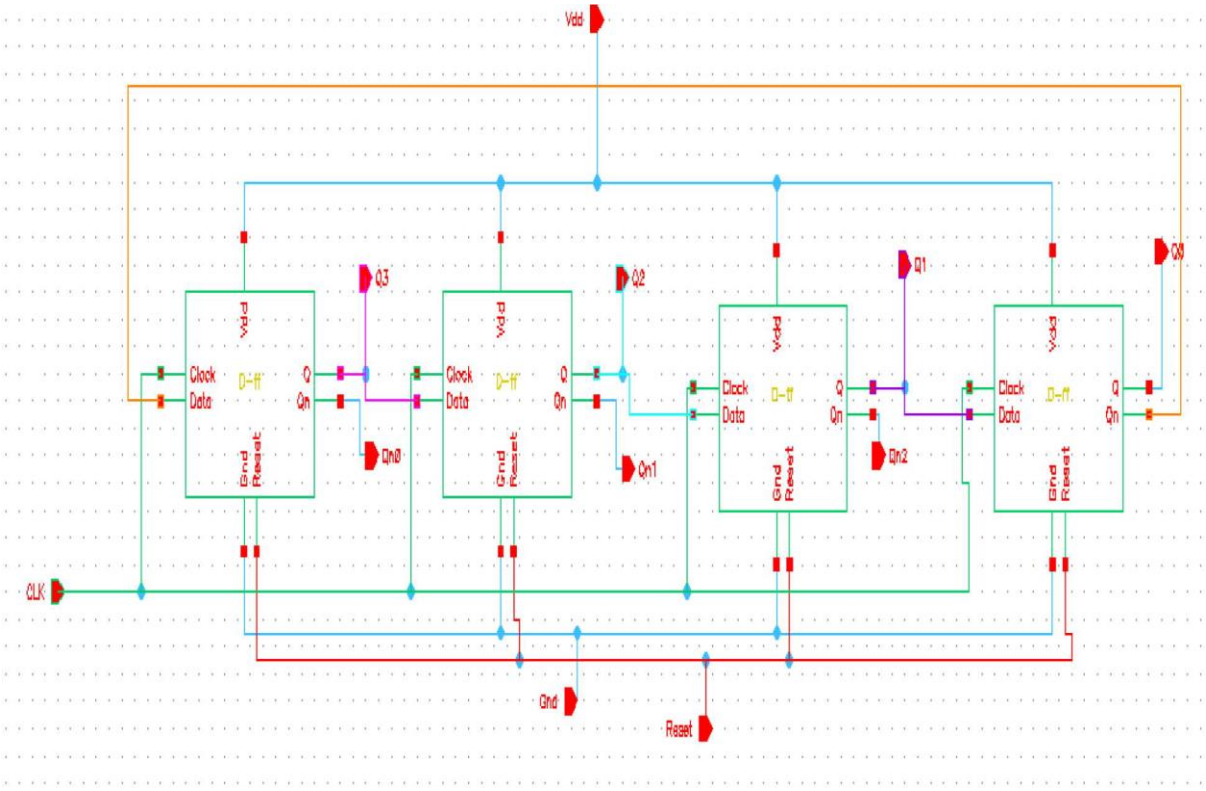

Figure 3: Proposed Johnson Counter

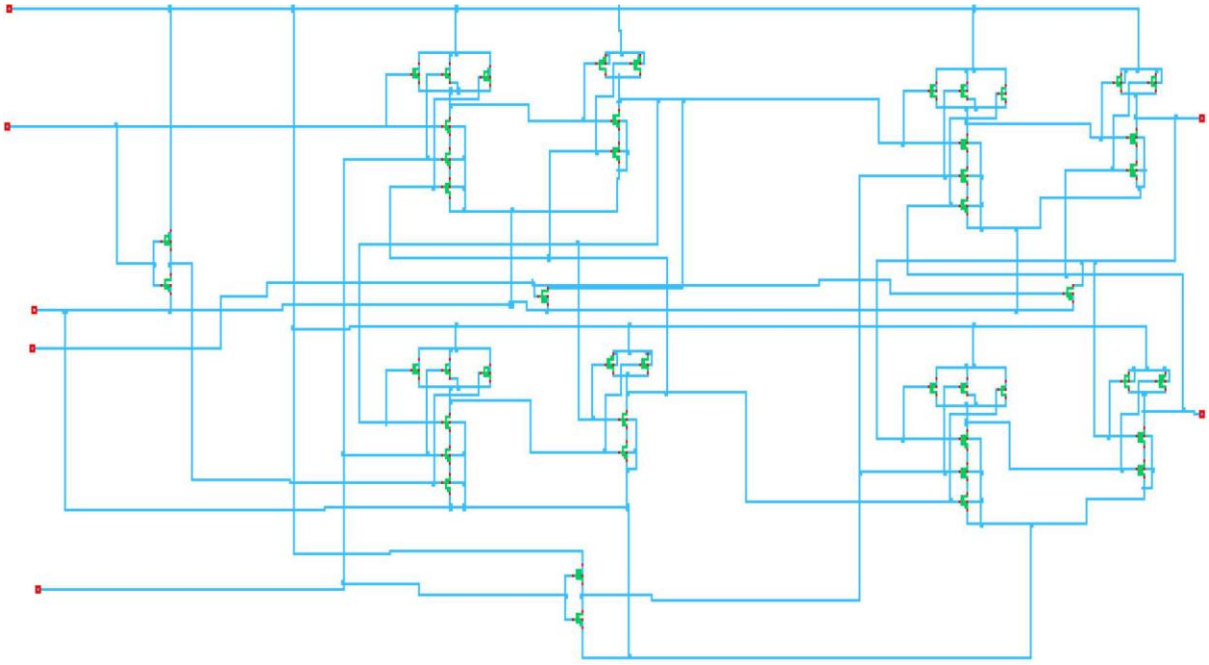

Figure 4: Conventional Master Slave D Flip- Flop

In the design, 4 instances of the created flip-flop cell are used in cascade where the input of a flip-flop is derived from the output of next most significant flip flop. The input of most significant flip flop is derived from the inverted output of least significant flip flop. There is a provision of same dock pulse to realize the functioning of Johnson counter. A common reset pulse is also connected to all the flip flops in parallel to reset the state of the counter to zero whenever required. A 4 bit Johnson counter using conventional master slave D flip flops is also designed and implemented. The conventional master slave D flip flop with 8 NAND gates and an inverter is designed using PMOS and NMOS of same specifications and is as shown in Fig. 6.

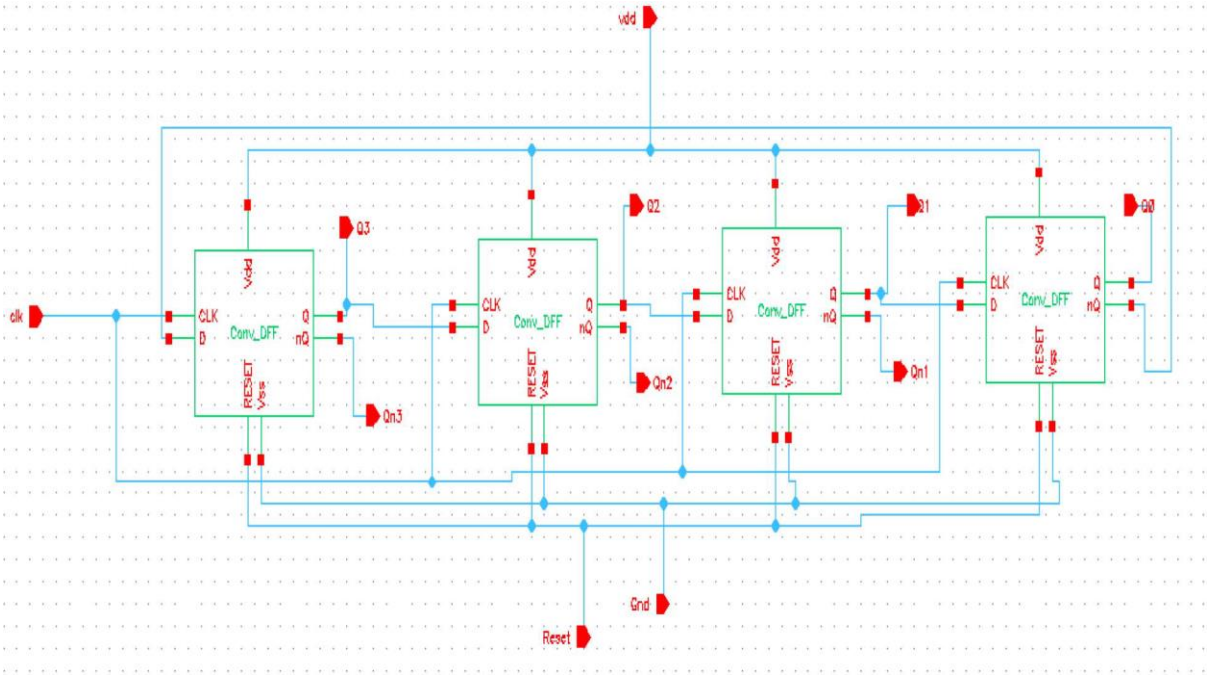

Figure 5: 4 bit conventional Johnson counter

The schematic shows the internal configuration of conventional master slave D flip flop in terms of NMOS and PMOS transistors. 2 input and 3 input NAND gates are realized and are then connected as per the gate level schematic design of conventional master slave D flip flop. A cell of this conventional D flip flop is created which is used to implement the design of 4 bit conventional Johnson counter as shown in Fig. 7. The schematic of 4 bit conventional Johnson counter is created in the similar manner as in proposed design. 4 instances of the conventional D flip flop cells are used and connected in shift register mode with the inverted output of least significant flip flop connected to the input of most significant flip flop.

V. RESULT SIMULATIONS AND DISCUSSIONS

Tanner EDA also gives the count of transistors used in the design Performance and comparative analysis of the proposed Johnson counter design with respect to the conventional design, in terms of power dissipation, delay and transistor count is done in Table 3. All the parameters are then graphically compared with the help of bar charts. Fig. 10 shows the comparison of the proposed counter with conventional counter in terms of power dissipation and delay.

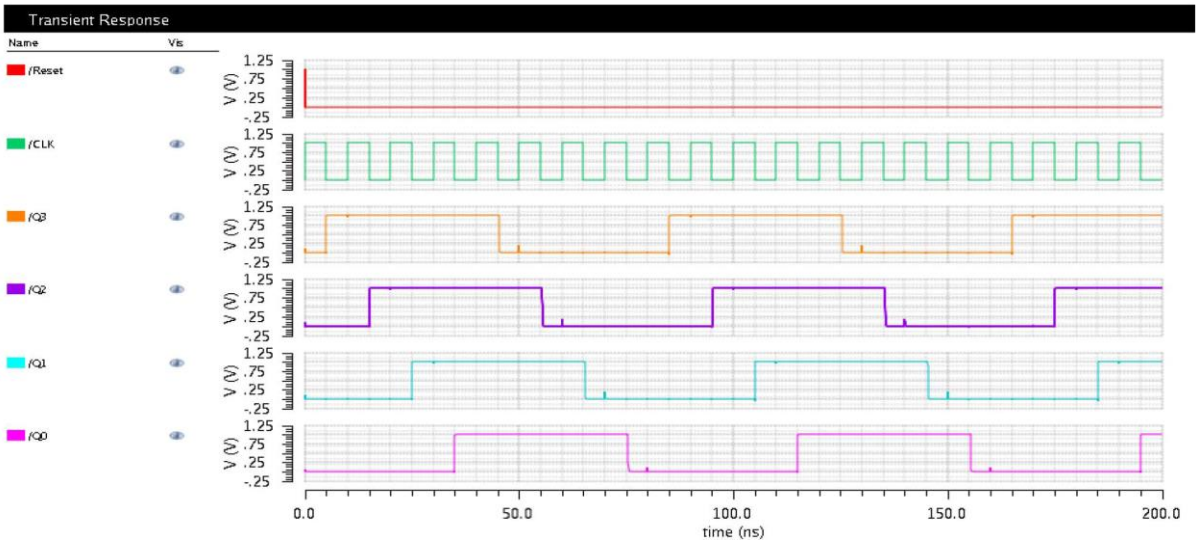

Figure 6: Transient Response of Proposed 4 Bit Johnson Counter

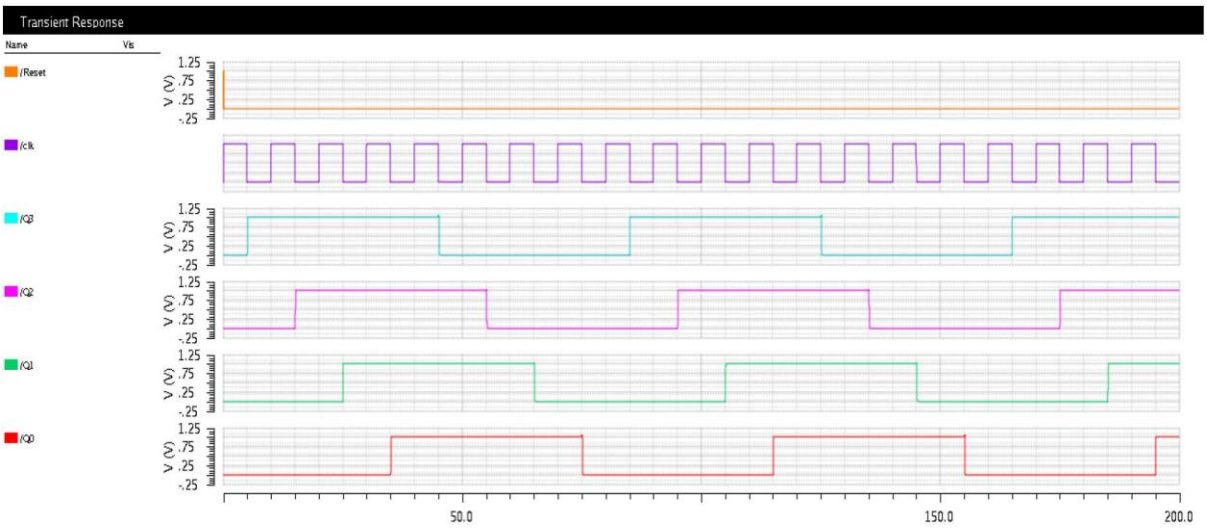

Figure 7: Transient Response of Conventional 4 bit Johnson Counter

TABLE 3: PERFORMANCE AND COST ANALYSIS

Design	Power Dissipation (nW)	Delay (ns)	Transistor Count
Conventional Johnson Counter	0.36618	0.0845	184
Proposed Johnson Counter	0.2079	0.04321	56

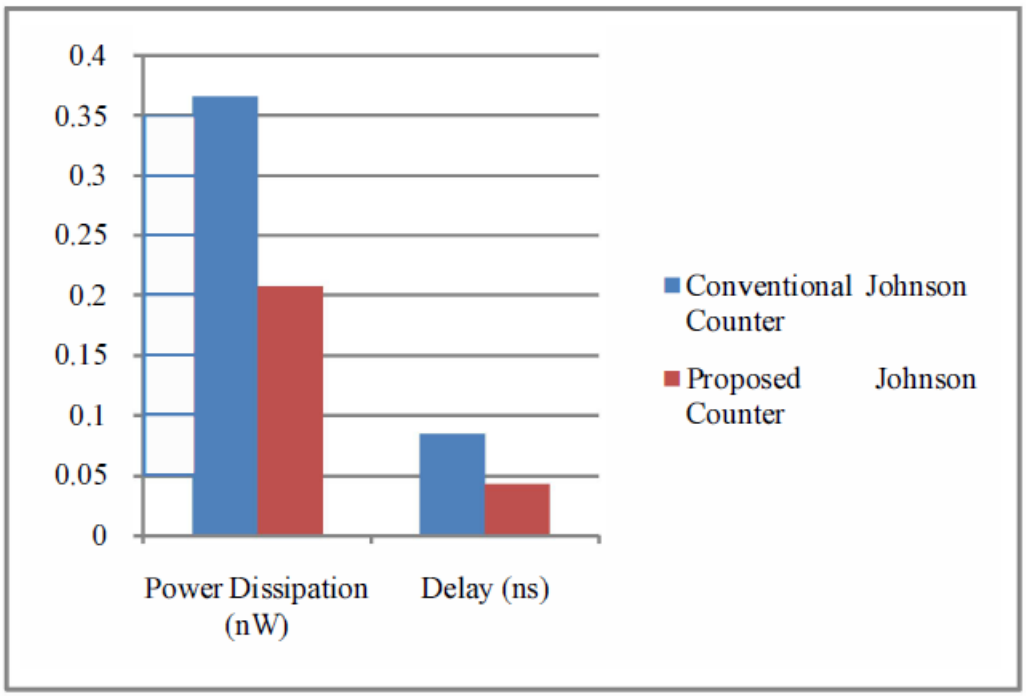

Figure 8: Comparative Analysis in Terms of Power Dissipation and Delay

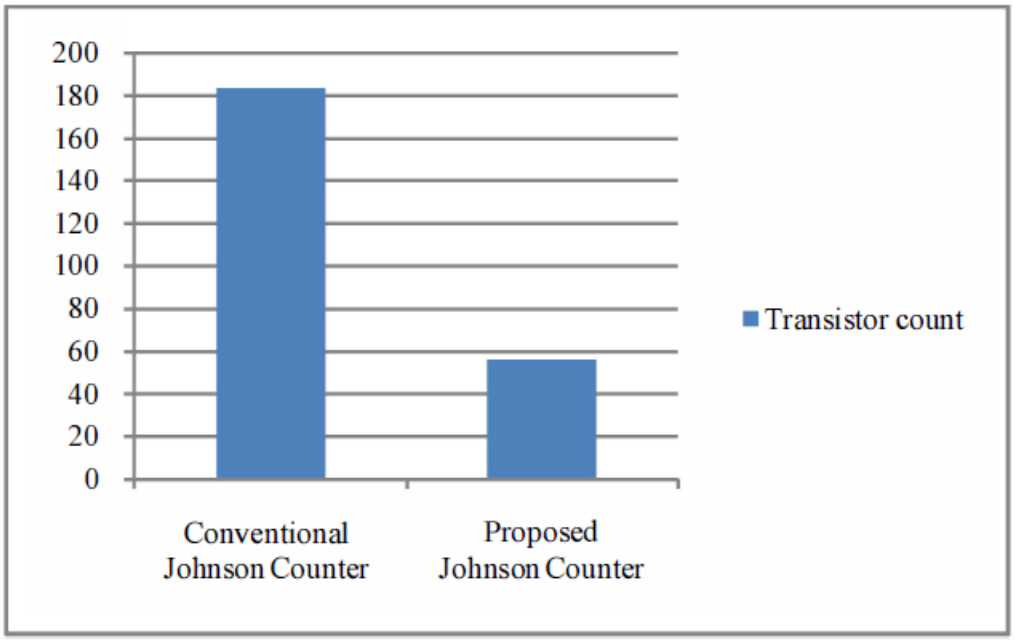

Figure 9: Comparative Analysis in Terms of Transistor Count

VI. CONCLUSION

To realize the negative edge triggered master slave D flip flop, a deployed flip flop circuit is designed which uses 14 transistors. Comparative analysis in terms of performance and cost is done against the conventional counter and proposed design. It is found to be 43.22 % of lesser power dissipation in the proposed design than conventional design. When compared to conventional design the transistor requirements in the proposed counter is 69.5 % lesser which makes it an optimized design in terms of area. The power dissipation in the proposed design has reduced to 0.2079 nW compared to 0.36618 nW in conventional design. The cost analysis of the two designs shows that the proposed counter requires 56 transistors compared to 184 as required in conventional counter which makes the proposed design highly cost efficient.

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