Optimization & Analysis Techniques of switched-capacitor DC-DC Converters

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Abstract- A switched-capacitor (SC) dc–dc converter's steady-state performance through evaluation of its output impedance. This analysis method has been verified through simulation and experimentation. The simple evaluation developed permits evaluation of the capacitor sizes to meet a parameters such as a total capacitance or total energy storage limit, and also permits optimization of the switch sizes subject to constraints on total switch conductance or total switch volt-ampere (V-A) products. These techniques allow comparison among several switched-capacitor topologies, and SC converters with conventional magnetic- based dc–dc converter circuits, in the context of various application settings. Significantly, the performance (based on conduction loss) of a ladder-type converter is found to be superior to that of a conventional magnetic-based converter for medium to high conversion ratios.

Keywords: Analysis, dc-dc converter, output impedance, switched capacitor

1. INTRODUCTION

This thesis is used to evaluate steady state performance of a switched capacitor dc- dc converter by determining its output impedance. This thesis builds up a circuit, which can be utilized to access both the converter proficiency and produce output as a component of load for an expansive class of SC converters.

This method created grants improvement of the capacitor sizes to meet a limitation. These improvements are done among several switched capacitor topologies. These optimizations at that point allow comparison among a few switched capacitor topologies, and correlations of SC converters with traditional magnetic based dc– dc converter circuits. The execution of a ladder type converter is observed to be better than that of a traditional boost converter for medium to high change proportions.

2. Switched Capacitor Converter Impedance Analysis

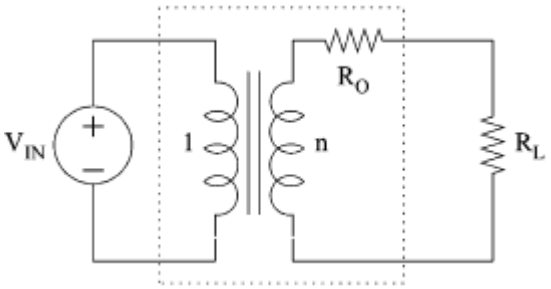

Figure 1. Model of an idealized switched capacitor converter

The converter shown in figure 1 gives a perfect dc voltage conversion ratio under no heap conditions, and all transformation losses are showed by voltage drop related with non-zero load current through the output impedance. The resistive output impedance represents capacitor charging what's more, releasing losses and resistive conduction losses. Extra losses because of short circuit present and parasitic capacitances, not withstanding gate drive losses, can be consolidated into the model. Be that as it may, they won't be considered here since these impacts are by and large application. Understanding picked up can be utilized to display impacts of parasitic capacitances. For the present, our point is to give a general examination analysis and design frame work.

Two-phase converters switch alternately between two configurations. Multiphase converters are outside the scope of this paper, but can be considered using similar methods. This thesis does not explain the basic fundamental topological conditions required to evaluate whether or not a specific circuit constitutes a well-formulated two-phase converter. Rather, the paper assumes that the circuits under consideration all have well-defined two-phase operation.

2.1 Slow Switching Limit Impedance:

For the slow-switching limit (SSL) impedance analysis, the finite resistances of the switches, capacitors, and interconnect are neglected. For the ladder network example of Figure 2, the charge multiplier vectors can be obtained through network analysis using Kirchhoff's Current Law (KCL). In this example, and in all other examples encountered by the authors, the charge multiplier vectors can be obtained by inspection. During phase 2 the charge from the input source flows into C4. That charge is transferred into C3 during phase 1. By considering alternating phases, the charge flow in each component can be found. In each of these charge multiplier vectors, the first component corresponds to the output charge flow, thus these two components must sum to one. The last component of each charge multiplier vector corresponds to the charge flow into the input source, and is non-zero during only phase 2 in this example.

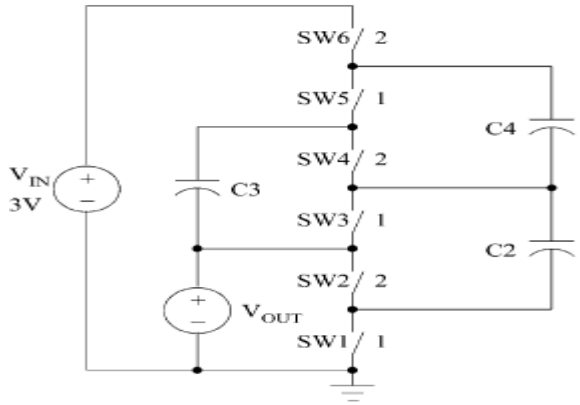

Figure 2. 3V to 1V ladder circuit

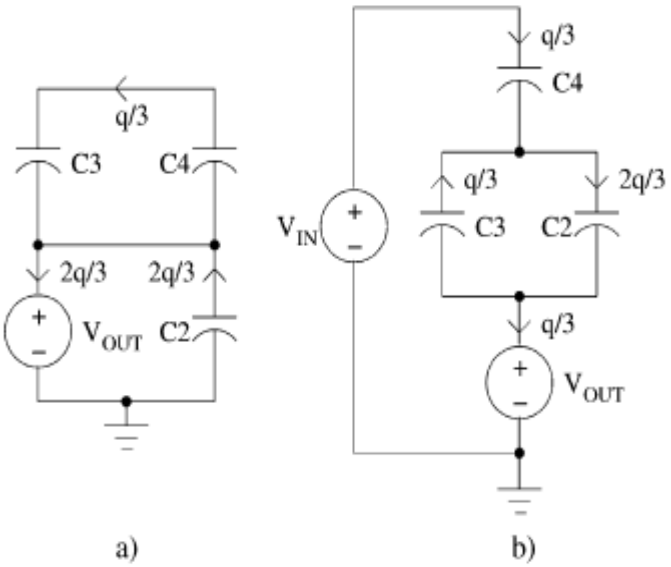

Figure 3. Charge flow in ladder converter (a) Phase 1 (b) Phase 2

2.2 Fast Switching Limit Impedance:

The other asymptotic limit, the fast switching limit (FSL), is characterized by constant current flows between capacitors. The switch on-state impedances and other resistances are sufficiently large such that during each phase, the capacitors do not approach equilibrium. The capacitor voltages are considered as constant in the asymptotic limit. In Resistive elements the circuit loss is related only to conduction loss.

While considering the FSL impedance, the duty cycle of the converter is important since currents flow during the entirety of each phase. A duty cycle of 50% is assumed for simplicity of analysis. Duty cycle differing from 50% can be included in the following analysis without much difficulty if another duty cycle is used. Additionally, only the on-state switch resistance is considered; other parasitic resistance [e.g., capacitor equivalent series resistance (ESR)] can be similarly incorporated into the model if desired.

For positive power flow (i.e., from the input to output source), the sign of each component of the vector indicates the direction of current flow with respect to the blocking voltage of a switch. When the switch conducts positive current while on and blocks positive voltage while off it indicates a positive quantity. This switch must be implemented using an active transistor. When the switch conducts negative current and blocks positive voltage and is suitable for diode implementation (if the forward voltage drop is tolerable) it indicates a negative quantity. For power flow in the opposite direction, the switch types reverse.

3. Component Optimization:

Given that all converter losses attributed to the capacitors and resistive switches can be reflected in the computation of a single real output resistance, it is now possible to minimize that output impedance by optimizing the components in order. Minimal output impedance corresponds to maximum efficiency for a given power delivered, and dually, corresponds to maximum power delivery for a given loss. The development of the slow switching limit (SSL) and the fast switching limit (FSL) impedance is done by optimality computations. The FSL output impedance should be minimized when optimizing over switches sizes.. The final design step is to choose a maximum operating frequency for which the parasitic losses are acceptable. The total capacitance and device conductance should to be balanced with the overall impedance meets the network output and the SSL and FSL impedances are balanced. The last advance guarantees that the total switch and capacitor sizes (and expenses) are limited for the expected power level.

3.1 Slow Switching Limit Capacitor Optimization:

The capacitor optimization uses a constraint that holds the total energy storage capability, summed over all capacitors, fixed to a constant total energy. The energy storage ability of a capacitor is identified with its rated voltage, as that controls its size and cost, not the most extreme voltage it sees during operation. Be that as it may, the capacitor's working voltage must be not exactly the rated voltage to keep away damaging the component, and ought to be near the rated voltage to accomplish great use of the device.

By optimizing the capacitors, the output impedance becomes corresponding to the square of the sum of the results of voltages and charge flows (V-A product) of every capacitor. The advancement can ensure the evaluation of a SC converter designed in a specifically way, particularly one with a large conversion ratio.

3.2 Fast Switching Limit Switch evaluation and sizing:

Like capacitors, the switches in a SC converter can be optimized, output dynamic performance increases. This optimization is carried out in the asymptotic fast switching limit where output impedance is directly connected to switch conductance. This optimization considers a duty cycle of 50%. The device VA product, added over all switches, is used as the economic evaluation in this technique. This V-A measurement related to a constraint on the $G\text{-}V^2$ product summed over the devices, for both discontinuous and integrated devices. Paralleling discrete switches increases total conductance, whereas placing switches in series increases voltage blocking while decreasing conductance. To improve voltage blocking with maintaining conductance constant, the number of devices required increases quadratically, motivating the $G\text{-}V^2$ metric.

4. Conversion of SC Converter Topologies:

A number of SC converter topologies exist; the advantages of each topologies have not been differentiated in a theoretical way. The various techniques are used to provide a evaluation comparison among various common SC converter configurations Step-up versions of the topologies are considered, as shown in Fig. 5, although step-down forms would give same results. In both the results the optimal output impedance for all configurations evaluated for a span of conversion ratios (represented by n).

All devices having same voltage rating must be assumed for performing the second comparison. The switches and capacitors are usually evaluated for the common voltage, in integrated applications using standard CMOS processes. The process is chosen such that this voltage rating corresponds to the maximum voltage seen on any device. However, the switches and capacitors can be rated differently from each other, i.e., if the highest-voltage switch is rated for 1V, a 1 V process would be used, even if some capacitors support a higher voltage.

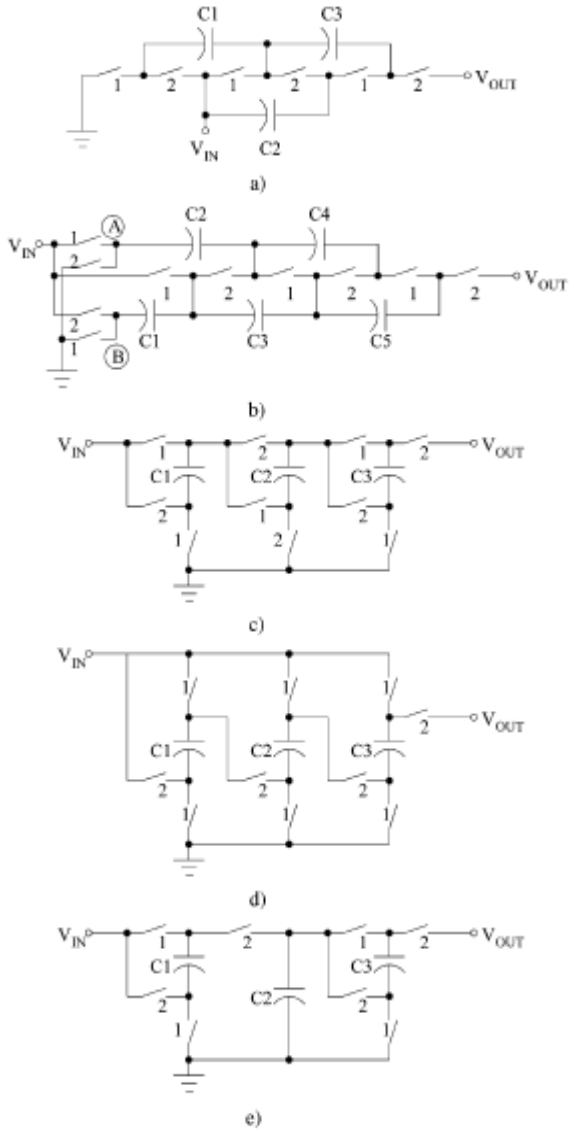

Figure 4. 5 step SC converter topology (a) ladder (b) Cock-croft-walton multiplier (c) Fibonacci (d) series-parallel (e) doubler

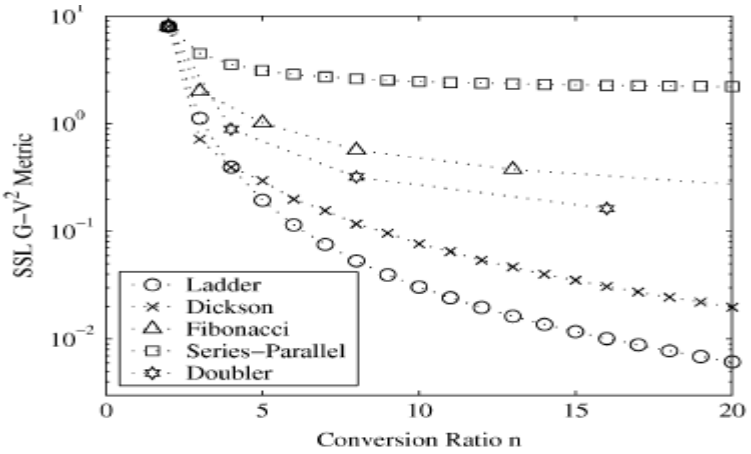

Figure 5(a). SSL evaluations measurement with optimal voltage devices

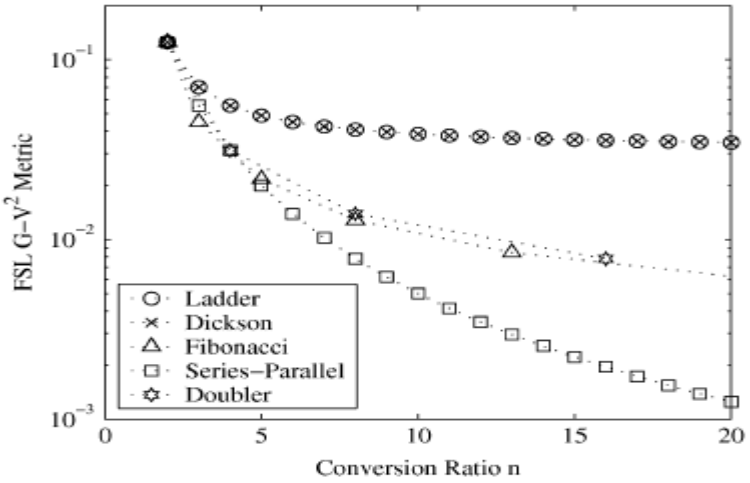

Figure 5(b). Fast Switching Limit performance scale with optimal voltage devices

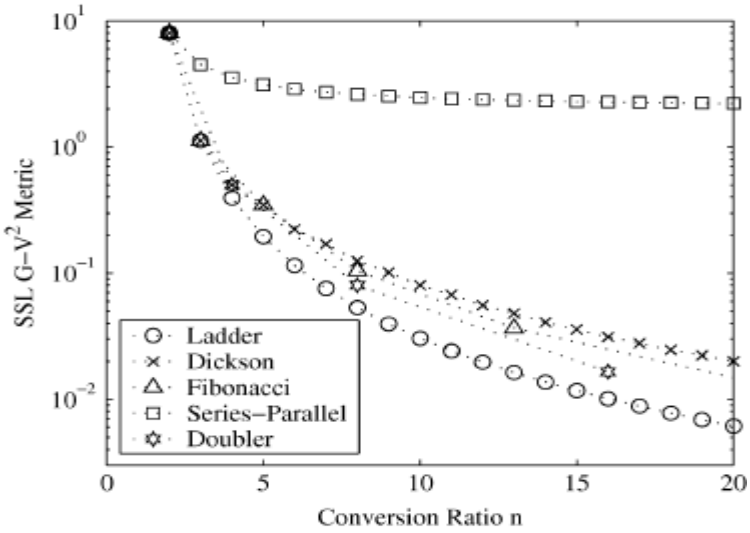

Figure 6(a). SSL performance metrics with single voltage devices

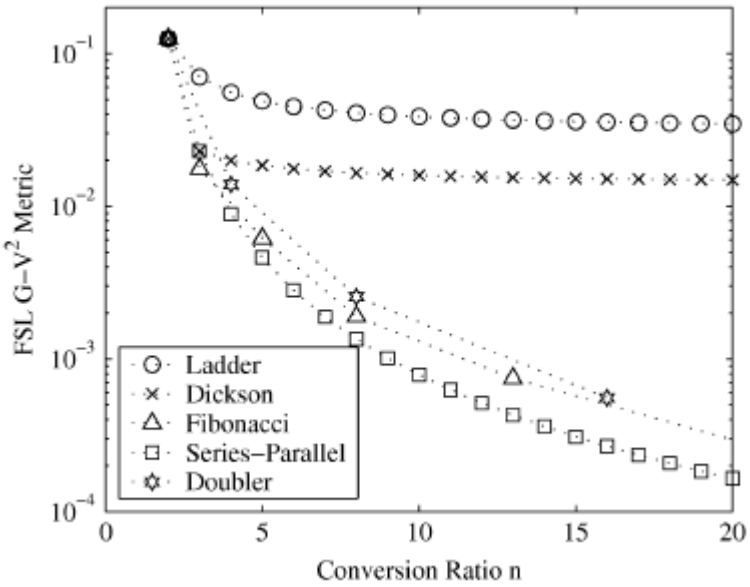

Figure 6(b). FSL performance metrics with single voltage devices

6. Verification by Simulation:

As this simulation method is found on ideal devices, circuit- level simulation, through SPICE or spectre is appropriate for verification of this analysis. In this simulation, Ideal capacitor and voltage-controlled resistances are used. Parasitics, meanwhile an significant analysis in real-world implementations, are not considered in this paper, and are not considered in the verification simulation. Over a wide span of switching frequencies, five step-up switched-capacitor converters have been simulated. By varying the switching frequency, both the slow switching limit and Fast switching limit output impedances can be evaluated and compared with those from the mathematical evaluations.

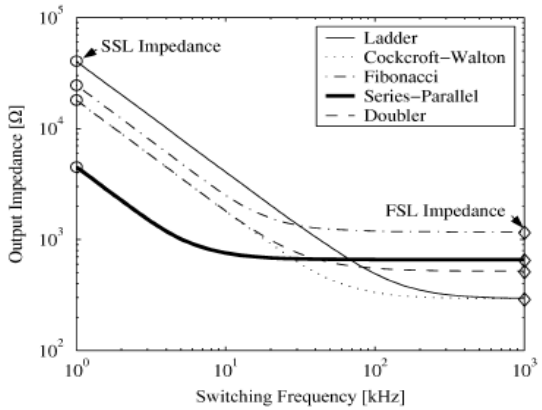

Figure 5. Simulated output impedances Vs Switching frequency

7. Conclusion:

Hence determined the evaluation of any switched-capacitor power converter using easily-determined charge multiplier vectors by presenting a analysis method. The semi conductor switches and capacitors were optimized to reduce the output impedance for various terms and constraints. Five individual converter configurations were selected for their effectiveness in utilizing capacitors and switches. This difference allows the use of an optimal configuration belonged to its application and implementation technology. Similarly, the evaluation (based on conduction loss) of a stair case-type converter was found to be far better than that of a standadard boost converter for medium to high conversion ratios.

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