Design Of Indirect Matrix Converter For Single Input-Dual Output Applications

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Abstract—This project presents a design of matrix converter with one ac input and two ac outputs. The presented topology is based on indirect matrix converter with nine-switch inverter using MATLAB simulation. With only three extra switches added with existing converter, the proposed converter can produce two sets of three-phase ac outputs, whose amplitudes, frequencies, and phases can appropriately be regulated. The features such as sinusoidal input and outputs, unity input power factor and minimum commutation count are all retained by the proposed topology, despite having an additional output.

Keywords- Carrier-based modulation, dual outputs, FPGA, indirect matrix converter (IMC), nine-switch converter

I. INTRODUCTION

AC-AC power converter are all over in practical applications Such as adjustable speed motor drives, wind generation system, electronic transformer, and many others among the plentiful ac-ac convert topologies available, the traditional back-back converter, comprising a common dc-link capacitor and two voltage source inverters, is frequently used. The main drawback of this topology is its requirement for a bulky electrolytic capacitor at its dc-link for filtering and short-ter energy storing purposes. This capacitor has always been the main the main source of premature failures, affecting converter reliability. Another shortcoming experienced by the back-back converter is its requirement for two bulky sets of three phase line, whose sizes would limit its compactness, when implemented.

Other than the back-to-back topology, different ac-ac matrix converters can be considered, including the direct matrix converter, indirect matrix converter (IMC), sparse ma-trix converter, ultra-sparse matrix converter, and others. These matrix converters can convert any three-phase input ac source to an ac output with controllable amplitude, frequency and phase. Without the intermediate dc-link capacitor, matrix converters, being “all-semiconductor,” are more easily packed to a smaller enclosure, which is probably their main attraction. It should however be noted that although matrix converters do not have any dc-link capacitor, the name “dc-link” is still frequently used with the indirect, sparse and ultra-sparse matrix converters. To illustrate why, the IMC shown in Fig. 1 is considered, where a fictitious dc-link is undeniably formed, after cascading the front-end current-source

rectifier (CSR) to the rear-end voltage source inverter (VSI). Although many matrix topologies have been proposed, they are mostly of the single-output type, therefore not suitable for applications like electric traction locomotives and elevators, where two (or more) motors need to be driven independently [12]. For the IMC shown in Fig. 1, the most straightforward solution is to use one rear-end inverter for each ac load, which means N inverters with $6N$ switches for N loads, where N is an integer. The resulting topology might unnecessarily be costly and bulky, since sharing of switches has not yet been properly considered. In fact, for the specific case of $N = 2k$ (or $2k + 1$) loads, the total number of switches can be reduced from $12k$ to $9k$ (or $9k + 6$), based on the nine-switch topological concept proposed in [13], [14], and redrawn in Fig. 2. Conceptually, the nine-switch inverter merges two six-switch inverters together by sharing three switches, therefore also has two three-phase ac outputs and a common dc-link. The shared switches are in fact the middle three switches (ST_2, ST_5, and ST_8) with them forming the first inverter with the upper three switches (ST_1, ST_4, and ST_7) and the second inverter with the lower three switches (ST_3, ST_6, and ST_9). More than two outputs can

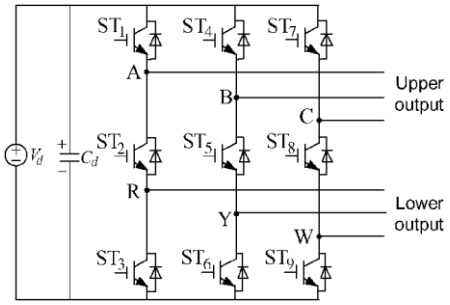


Fig. 1. Dual output nine-switch inverter.

also be catered by paralleling more nine-switch inverters and six-switch inverters with the latter mainly needed only when the number of outputs demanded is odd ($2k + 1$).

However, application of the nine-switch inverter is less than perfect at present due to its higher rated dc-link capacitor, needed to produce the same ac output voltages as per the case of two individual inverters. The reason is mainly linked to the fact that the sum of modulation indices of its two outputs must be lesser or equal to unity when their frequencies are different. [15], [16] advanced the concept by adding a Z-source network to the dc-link of the nine-switch inverter to introduce an additional degree of buck-boost freedom to its dual outputs, but it still requires bulky and higher rated passive components and in fact is worsened since two inductors and two capacitors are now present. Therefore, bulky volume and relatively low reliability are the presently unsolved shortcomings of existing nine-switch inverters.

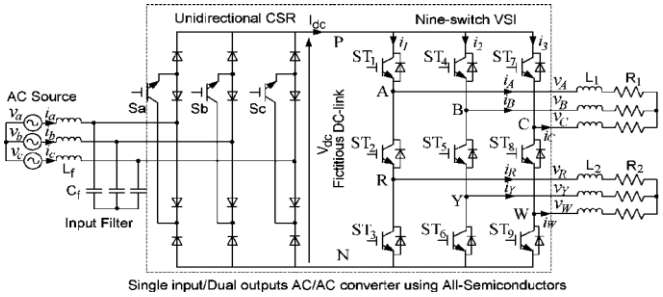


Fig 2. Topology of proposed matrix converter

To firmly remove passive components from its dc-link, the idea of applying the indirect "all-semiconductor" matrix con-version concept to the nine-switch inverter is proposed here. The resulting topology still has dual outputs but can better match industrial conditions, where the primary electrical supply is ac and unity power factor operation is commonly sought for. Modulation scheme for the new single-input/dual-output matrix converter would certainly be more complex, particularly if features like sinusoidal input and outputs, unity power factor and minimum commutation count have to be achieved simultaneously. This complexity is resolved in this paper with full mathematical details provided for validation. Hidden conceptual details for easier implementation, while producing the correct modulation state sequences, are also discussed before being verified in simulation and experiment together with other findings.

II. SINGLE-INPUT/DUAL-OUTPUT MATRIX CONVERTERAND ITS OPERATIONAL PRINCIPLES

A. . Topology

As mentioned above, the proposed matrix converter is based on the indirect matrix converter shown in Fig. 1 and the nine-switch inverter shown in Fig. 2. If regeneration capability is expected, the front-end CSR of the matrix converter needs 12 switches in total, as illustrated in Fig. 1. For applications where only unidirectional power flow is required, the ultra-sparse matrix converter with a three-switch CSR can be used instead, which in fact is the topology based upon for the following analysis and verification, because of its simplicity. The concepts presented are certainly applicable to the bidirectional case, too.

Upon cascading the mentioned two entities together, Fig. 3 shows the resulting proposed matrix converter without any passive dc-link component. Only 12 switches are needed in total to form one input and two outputs with several operating scenarios possible with its dual outputs, identified as same frequency, same amplitude, different frequencies, different am-plitudes or a combination of them. These operating modes must be considered comprehensively, together with their associated fictitious dc-link current values, before a proper modulation strategy can be formulated for achieving sinusoidal input and outputs. Further discussion on it will be presented shortly in the section focusing on modulation theories.

B. Operational Principles

Because of its direct cascading basis, operational principles of the proposed matrix converter can be analyzed by study-ing its entities separately, before coordinating them later for optimal performance. Beginning with the front-end CSR then, two of its three switches must alternately be switched on to bring forth one of the nearest two space states surrounding the input current reference phasor, which also is the source voltage phasor for unity power factor operation. To illustrate, the vector diagram and reference phasor in Fig. 4 are drawn, which when transferred to the time domain, gives rise to those variations shown in Fig. 5. The applied dc-link voltage V_{dc} would then be the vertical length measured between any two waves in

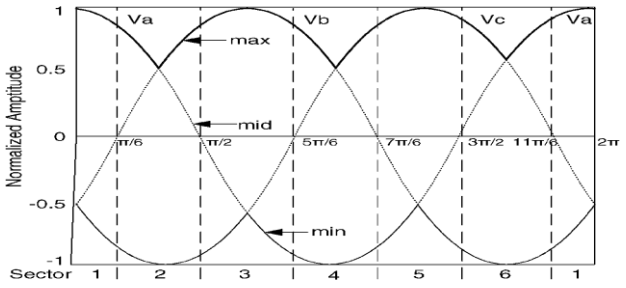


Fig 3.Six intervals of CSR input voltage waveform

TABLE I. Table Type Styles

Switching State	ST_1	ST_2	ST_3	V_{AN}	V_{RN}
1	1	1	0	V_{dc}	V_{dc}
2	0	1	1	0	0
3	1	0	1	V_{dc}	0

depending on which two CSR switches are turned on. Vdc can also be zero, if only one CSR switch is turned on, but this null state is usually not considered since it does not lead to maximal converter output. Vdc will then vary between vab and vac only, when in sextant 1 ($-\pi/6$ to $\pi/6$) of the vector diagram. The remaining voltages assumed by it are listed in Table I for the other five possible sextants. Putting and Table I together would then clarifies that the fictitious dc-link voltage applied to the rear-end nines witch VSI is not constant, but varies across sextants. This is unlike the conventional nine-switch inverter where a constant source voltage is usually applied. Modulating conditions of the nine-switch VSI here must therefore be modified accordingly to retain its sinusoidal outputs. This will be discussed in a later section focusing on modulation theories. For now, the middle shared switches of the nine-switch VSI are analyzed to check on how they limit the inverter operation. Taking ST2 in Fig. 3 as an example, turning it off would force the other switches in the same phase-leg, ST1 and ST3, to turn on, so as not to float any output. On the other hand, turning ST2 on would demand that only ST1 or ST3 can be turned on to avoid shorting the dc-link, while yet not float any output. Summarizing these constraints then leads to those three switching states per phase-leg shown in Table II, which together with Table I, governs the switching process of the overall matrix converter. For an illustration of how the states can be combined, Fig. 6 is drawn with only the ON switches and a typical current flow path shown for better clarity. This is however only one scenario at an instant in time, whose orientation would change when a new state is entered or when a phase current reverses its direction, as time progresses.

MODULATION AND SINUSOIDAL INPUT/OUTPUT PROOF

Modulation of matrix converter using space vector theory has long been established, and is known to have the advantage of flexible control over all its chosen space vectors, but at the expense of high computational burden and a sizable lookup table In contrast, carrier-based modulation introduces simplicity, but has no controllability over its auto-sequencing of states. Its simplicity has recently attracted the attention of some researchers, who have successfully applied carrier-based modulation to matrix converter. Because of this recent interest, analyses presented below are biased toward the carrier-based approach, but would still be valid for a space vector system since they share the same theoretical bases.

A. Modulation of CSR

As mentioned earlier, the front-end CSR imposes a selected input line voltage across the dc-link of the rear-end nine-switch inverter. When in sextant 1, the imposed line voltage would either be vab or vac, depending on whether the nearest active state

SC6 or SC1 is chosen, as reflected in Table I. The nearest two active states are in turn chosen based on which sextant the current reference phasor (or grid voltage phasor for unity power factor operation) is residing. Regardless of which two states are chosen though, their combined effects are to clamp one switch to a dc rail and modulate the other two switches alternately to the other dc rail. For the present two states of SC6 and SC1, the clamped switch to the positive dc rail is Sa, while the modulated switches to the negative dc rail are Sb and Sc. Defining (1) as the input, duty ratios of the modulated switches Sb and Sc.

B. Modulation of VSI

Carrier-based modulation of a traditional six-switch VSI with a fixed dc-link voltage is well known, and can be done simply by comparing three balanced sinusoids with a common triangular carrier. Applying it to two individual VSIs is straight forward too, since it just means duplicating another set of independent three-phase sinusoids and performing the same carrier comparison. Such independent duplication is however not directly applicable to the nine-switch VSI, because of its constrained phase-leg switching states listed in Table II. To ensure that only the allowed switching states are produced, modulating references of the upper terminals must always be placed above those of the lower terminals while using just one carrier Illustrations can be found in Fig. 8 with the two references per phase having either the same common frequency (CF mode) or different frequencies (DF mode). The references are clearly well separated vertically with no point of intersection noted between them, so as to avoid unwanted switching states and their accompanied volt-sec error. For the case of CF mode shown in Fig. 8(a), the criterion of clear separation is more correctly interpreted as a phase-shift constraint, limiting the maximum modulation indices of the references. In general, the following trend is a smaller phase-shift leading to larger modulation indices that can eventually reach a maximum of unity each (or 1.15 if triplen offset is added) when the phase-shift drops to zero. Such phase-shift constraint is, however, not felt during DF mode shown in Fig. 8(b). Rather, a strict amplitude constraint is imposed to the DF mode, which effectively limits its sum of modulation indices for its two references to be lesser or equal to unity (or 1.15) under all circumstances. Upon understanding the constraints and placing the references appropriately, they can next be compared with a single triangular carrier, but unlike traditional VSI control, the carrier for matrix modulation has variable rising and falling slopes. Modulating references are also no longer sinusoidal, after adding appropriate triplen offsets and compensating for dc-link variation. Both modifications are addressed hereon, but before proceeding ahead, it might be helpful to clarify how the references and carrier are related to the switches of the rear-end nine-switch VSI drawn in Fig. 3. For that, the variable-slope triangular carrier shown in Fig. 9, and the first phase-leg in Fig. 3, comprising ST1 to ST3, are considered as an example. In this example, the references per phase in Fig. 9 are intentionally drawn as horizontal constant lines in the single carrier period considered, which certainly is appropriate because of the usually much higher carrier frequency assumed.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The proposed single-input/dual-output matrix converter was preliminary verified in simulation using Matlab/Simulink and the PLECS power electronic libraries. Simulation was planned such that it used the same parameters as the final implemented hardware, whose values are listed in Table III. The experimental load resistances are slightly reduced to cover the inductor losses and switch conduction losses. For comprehensiveness, both CF and DF modes were tested using the carrier-based modulation scheme shown in Fig. 11. Experimentally, the scheme was im-plemented using a combination of dSPACE DS1103 controller card and Xilinx Vertex-II Pro XC2VP30 FPGA evaluation card (FPGA stands for field programmable gate array). The dSPACE card was tasked to synchronize with the three-phase input voltages, and identify the sextant in which the reference CSR phasor was residing. This information was passed on to the Xilinx card, whose external oscillator frequency of 100 MHz was adequate for

creating the 5-kHz variable-slope triangular carrier and the final driving signals for the overall matrix converter.

A point to note with the experimental setup is that it can be simplified to lower cost. One possible suggestion is to replace the expensive dSPACE card with a lower end 8-bit processor. External logic device is necessary, but rather than FPGA, the cheaper erasable or complex programmable logic devices (EPLD or CPLD) can be used in place. In spite of the options available, the setup assembled here is still considered as the most flexible for rapid high-end control verification, which indeed is the follow-up attempt, after verifying topological and modulation thoughts in this paper.

A. CF Mode

Figs. show simulation results obtained under CF mode, during which the upper and lower modulating references are set indifferently to 50 Hz, while their modulation indices are set to 0.8. The observed input currents in Fig. 13 are undeniably three-phase sinusoidal with an amplitude of 3 A. The fictitious dc-link voltage and current are also observed to vary according to expectation with six pulses per fundamental cycle for the six different sextants Fig to show the modified modulating references per phase, sinusoidal upper and lower output currents with peak amplitudes of 3.1 A and 1.6 A, respectively. The second output current is approximately half of the first, which certainly is correct, since the upper and lower modulation indices were set to the same value of 0.8, while the second load was configured to be twice bigger than the first in terms of impedance value.

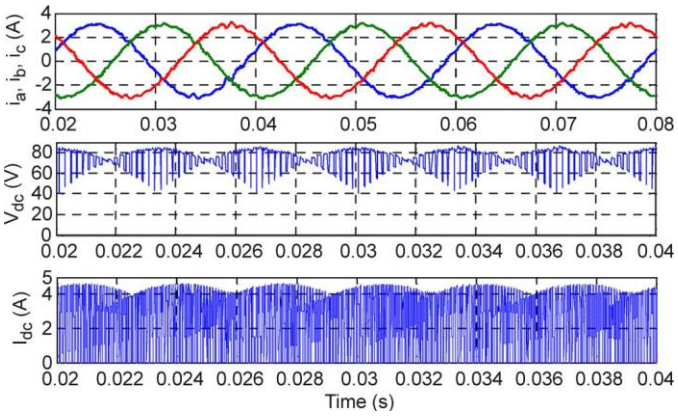
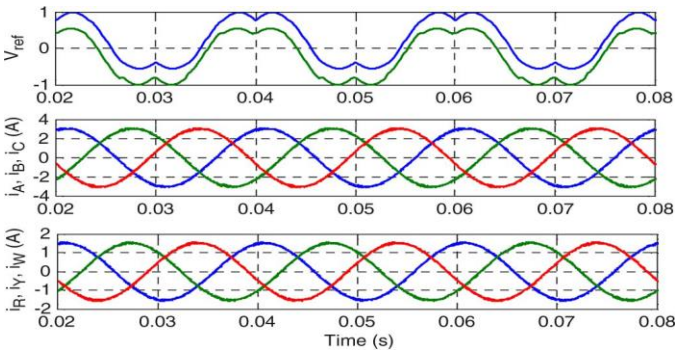


Fig. Simulation results in CF mode showing three-phase input currents ,fictitious dc-link voltage and current from top to bottom.



Fig, Simulation results in CF mode showing modulating references per phase, upper and lower three-phase output currents from top to bottom.

The corresponding experimental results under CF mode with Fig showing the in-phase input phase voltage and unfiltered current. It is certainly the unity input power factor but no longer so when the filtered input current is considered. The slight phase lead of the filtered input current, when measured with reference to the fundamental component of the unfiltered current, is contributed by the second-order input filter, which has long been associated with existing matrix converters. Fig. 16 next shows the experimental fictitious dc-link voltage and current over half a fundamental cycle while Fig. 17 shows the line voltages and currents of the dual VSI outputs with the same current peaks of 3.1 A and 1.6 A observed. In Fig. 17(c), the output currents are redrawn in one plot to show their phase and amplitude relations. The same phase relation is also applicable to the two fundamental output voltages, since the same resistive to inductive load ratio is maintained at both output terminals (see Table III). The second load is, however, twice bigger in impedance values, which when multiplied with its current, would lead to both fundamental output voltages having the same amplitude.

B. DF Mode

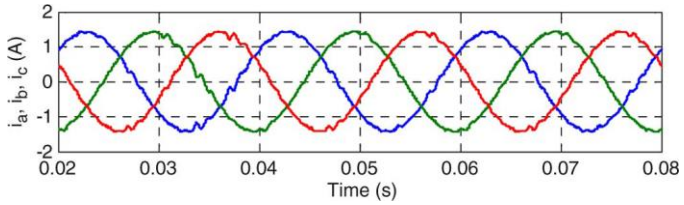


Fig. Simulation results in DF mode showing three-phase input currents.

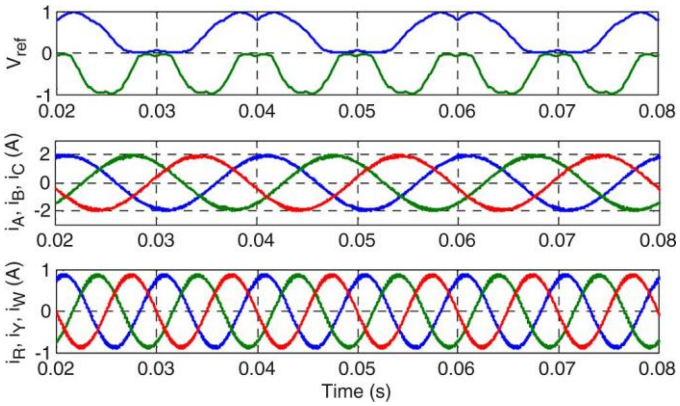


Fig. Simulation results in DF mode showing modulating references per phase, upper and lower three-phase output currents from top to bottom.

Testing was performed next under DF mode with the upper and lower modulating references set to 50 Hz and 100 Hz at the same modulation index of 0.5. The sum of modulation indices is then at its maximum of unity to avoid reference crossover, while yet utilizing the fictitious dc-link fully. With these parameters introduced, Fig again shows that the input currents are three-phase sinusoidal with an amplitude of 1.4 A. Fig shows the modified modulating references per phase, three-phase sinusoidal upper and lower output currents with amplitudes of 2 A and 0.9 A, respectively. These results agree well with theories and lead to confidence with the experimental testing, whose results are shown in Figs. Features noted from these experimental figures are in agreement with those discussed in Section IV-A, except that the outputs here have different frequencies and lower amplitudes,

which are caused by the imposed limit on modulation indices. DF mode of operation is thus also proven.

V.FUTURE ENHANCEMENT

This paper presents a compact three-phase single-input/ dual-output matrix converter, whose implementation uses only 12 switches, if only unidirectional power flow is demanded. The converter can be controlled by a variable-slope carrier modulation scheme, whose mathematical formulation has proven sinusoidal input and outputs. Other features like unity input power factor and minimum commutation count are also achievable and have already been proven in simulation and experimentally for both CF and DF modes.

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