Implementation of Symbol Synchronizer using Zynq Soc

M. Malavika[1], P. Kishore[2]

[1]M.tech Student, Department of Electronics and Communication Engineering, VNR VJIET,

[2]Assistant Professor, Department of Electronics and Communication Engineering, VNR VJIET,

[1]maratimalavika@gmail.com, [2]kishore_p@vnrvjiet.in

Abstract

Among the available Digital Modulation Techniques (QPSKFSK and QAM,BPSK etc), BPSK or Binary Phase Shift Keying/ QPSK or Quardrature Phase Shift Keying has desirable features for SDR SATCOM applications. The hardware design of Digital Signal Processing (DSP) based Symbol Synchronizer is developed for on board Telecommand System. It is designed and integrated with BPSK demodulator to recover the clock. The most suitable algorithm for this implementation is Gardner Algorithm. It contains all the functions necessary for a first-order, closed loop synchronizer. The Gardner based Symbol sybchronizer megafunction is fundamentally a digital phase locked loop (DPLL). The synchronizer is designed to provide phase lock between an internally generated data clock and an input data stream. At first this algorithm will be implemented in MATLAB/SIMULINK. Later the same algorithm will be implemented on to the FPGA using VIVADO/ISE tools. The whole design is accommodated on a Zynq Soc-FPGA.

Keywords: BPSK, QPSK, DSP, DPLL, SDR and SIMULINK.

1. Introduction

As a requirement of SDR (Software Defined Radio), digital signal processing (DSP) has become a preferred choice for implementation of communication systems, instead of traditional analog signal processing. Thus the sophisticated signal processing tasks, such as error control coding, synchronization, equalization, power control, channel estimation and so on, are all performed on the SDR based platform. Figure 1.1. shows the DSP functions in an SDR based receiver.

The hardware implementation of an SDR based communication system can be realized by means of semiconductor technology. In the early days, application specific standard parts Antenna Y RF to IF Translator ADC Digit: (ASI Digital Mixer Digital Local Oscillator (ASSPs), application specific integrated circuits (ASICs), digital signal processors (DSPs) and general-purpose microcontroller were the main solutions of building an SDR platform. During the last decade, field programmable gate array (FPGA) that can offer both high performance and flexibility has become the mainstream among these technology solutions, to meet the design requirement for ever increasing complexity of communication systems.

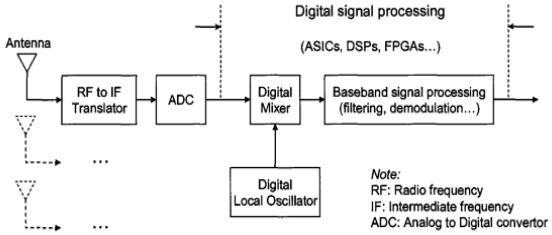

Figure 1.1. Digital signal processing in SDR based receiver

One of the challenging tasks in a communication system is carrier and symbol timing recovery. A large amount of time is spent solving these problems, and frequently a large amount of hardware and software in a SDR is dedicated to synchronization.

2. Gardner Timing Error Detector

The idea behind the Gardner algorithm is to find the zero-crossing point in the output of the interpolating filter. If the current timing estimation is too early from the correct timing, then the timing offset is positive, which indicates that the timing should be advanced. And vice versa, if the current timing is too late, then the timing offset is negative, which means that the timing should be slower. The important point is that the Gardner TED does not require any extra information except the current samples to work (i.e., it is non-data-aided TED). Also, Gardner showed that for a fixed timing offset, the timing error is independent from any carrier phase rotation. These properties make the Gardner TED perfectly suited for high speed QAM applications.

The algorithm was proposed by Gardner to detect timing error that uses only two samples per symbol, and one of the two samples is used for symbol detection. The Gardner TED operates upon samples and generates one error sample e[l] (i.e., timing error) for each symbol. The index l refers to symbol number. The strobe values of the lth symbol are denoted by yI[l] and yQ[l]. The pair of samples lying midway between the (l−1)th and the lth strobes are denoted as yI[l−1/2] and yQ[l−1/2]. The detector's algorithm is based on the following formula:

$$e[l] = y_I[l-1/2](y_I[l-1] - y_I[l]) + y_Q[l-1/2](y_Q[l-1] - y_Q[l]) \quad (1)$$

Timing error gives information about the current timing offset, which is denoted by τe[l]. Let reconsider an example system that uses 4 samples per symbol (i.e., U = 4). The input of the Gardner TED is denoted as y[k]. Then one symbol (index l) is detected in every 4 consecutive samples (index k). Gardner TED uses only 2 samples per symbol so the 2 other samples are not needed to compute timing errors. The timing error e[l] is negative which indicates that the current timing offset τe[l] is negative and the samples marked with an asterisk should be slower.

For alternative symbols±1 with 4 samples per symbol, timing error is exactly 0 for samples at correct timing and at every computation, as midway samples are always equal to 0. The Gardner TED still works for random symbols because the expected value of timing error at correct timing is 0. This idea is illustrated by evaluating the input-output characteristic of the detector, or S-curve. Timing error is now presented as a function of timing offset. Note that this is different from Eqn (2.27) where the timing error is a function of time as it is digitally computed at

every symbol time. Figure 2.16 shows the theoretical S-curve for PAM (Pulse Amplitude Modulation) using the SRRC pulse shaping filter with a roll-off factor β = 0.25. The curve shows expected timing error for timing offsets varying in one symbol period range.

The S-curve in Figure 2.16 illustrates that the expected timing error has the same sign as timing offset and is exactly equal to 0 for correct timing (i.e., τe[l] = 0). Note that the Gardner TED requires the transition of signal from positive to negative or vice versa. If there is no transition (no zero-crossing), no timing information is available. The timing error is then used as the control information for the timing recovery loop to find the correct timing.

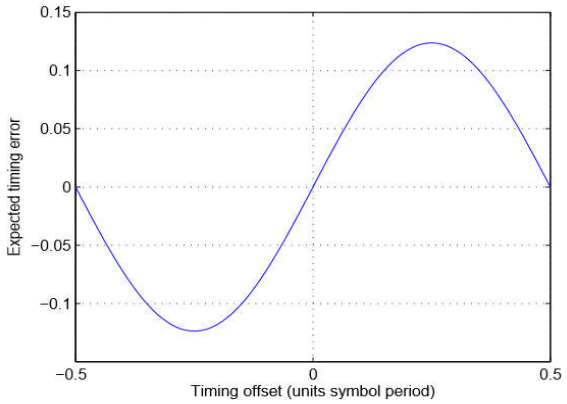

Figure 2.1. Theoretical S-curve of the Garder TED for binary PAM

3. System Design

A model for a typical digital communication system can be categorized into three fundamental parts, transmitter, channel and receiver. The information source for such a system is in the form of binary data, i.e., "0" and "1". In the beginning of transmission, the binary data is source encoded or compressed to eliminate the redundant information as much as possible. Then channel coding, which is known as error control coding, is applied to introduce some controlled redundancy into the data stream for the purpose of protecting against channel induced errors. At the same time, every certain number of data bits are grouped together preparing for the digital modulation. In the end of transmitter, those bit groups are modulated to digital symbols, and mapped onto analog waveform for transmission over physical channel.

In practice, a channel could be a wire, a fiber optic cable, free space, or a variety of other models. Each of these has different characteristics affecting the transmitting signal differently. Normally, two major sources of channel interference have to be considered in a wireless environment, which are multipath fading and noise. While the former is a result of scattering, refraction, and reflection from terrestrial objects, the latter is mainly due to the thermal noise existing in front end receiver electronics, such as band pass filter. Both of them cause signal amplitude and phase distortion. Furthermore, the noise can be model as an additive white Gaussian noise (AWGN) channel which has a uniform power spectral density and a Gaussian distributed amplitude. Various other sources of channel corruption exist, and have to be taken into account when necessary. These factors include the movement between transmitter and receiver, number of antennas, number of users, and so on.

The ultimate task of receiver is to extract the original transmitted data from the received signal that is corrupted by the channel. In order to do so, all the coding, modulation and signal processing performed in the transmitter should be reversed at the

receiver. To accomplish this task, knowledge of channel characteristic, original data clock and other information of transmitted signal are always required. The performance of the system is qualified by how much of the transmitted data can be successfully reconstructed by the receiver. This is measured with respect to the error probability by comparing the original data with the reconstructed data. The probability depends on many factors including modulation schemes, channel types, signal to noise ratio (SNR) and so forth. In order to achieve an acceptable error level, channel and transmitted signal information should be understood as much as possible in the receiver.

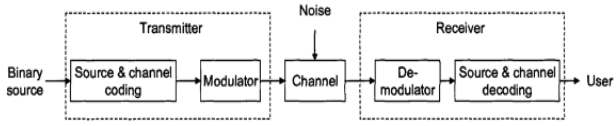

Figure 3.1. Basic components of a digital communication system

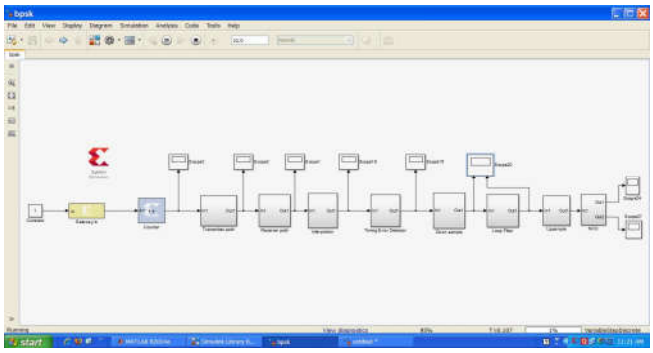

Figure 3.2. Simulation blocks of the Modem

4. Symbol Timing Recovery

4.1 Interpolator

In our design, the matched filter and interpolation filter are rolled into a same stage where a so called interpolated matched filter is used for the timing adjustment. The new matched filter is actually an upsampled version of original matched filter, and each interpolant between each sample can represent a different timing offset with respect to symbol interval. When polyphase structure is further applied to the filter design, each sub filter corresponds to a different timing offset. In other words, selecting the correct sub filter means making the correct timing adjustment.

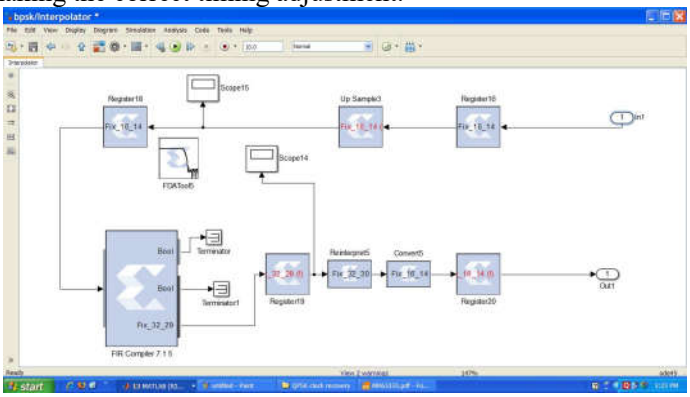

Figure 4.1. Simulation Blocks of Interpolator

4.2 Timing Error Detector

Timing error detector (TED) computes the timing error based on the comparison of current sample timing and estimated symbol timing. Two common structures exist for timing detection using PLL technique, that are Decision Directed (DD) structure which uses the data decision to perform detection, and Non-data Aided (NDA) structure, where the detection is independent of the data decision.

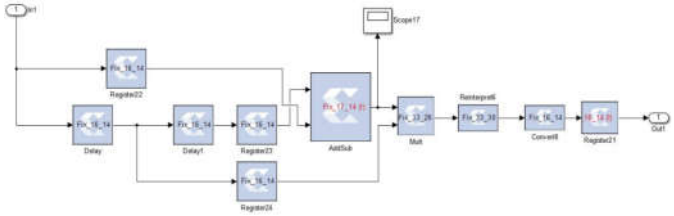

Figure 4.2. Gardner's timing error detector

4.3 Loop Filter

The loop filter in carrier recovery loop is a proportional-integral UR (Infinite Impulse Response) filter, where the proportional path tracks the phase error, and the integral path tracks the frequency error. It provides a filtered phase error signal with high precision for NCO processing, and normally 32 bits are required.

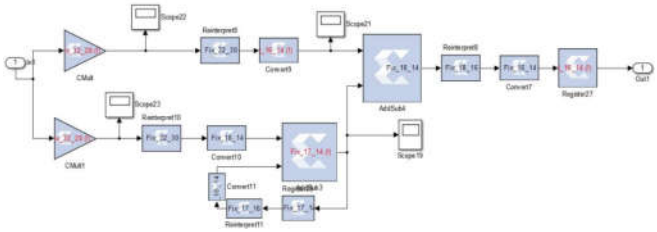

Figure 4.3. Digital Loop Filter

4.4 NCO

The task of NCO is to determine basepoint index mk and fractional interval μk. As mentioned before, the former represents the correct set of signal samples, and the latter indicates the correct set of filter coefficients. The NCO is actually a decrementing modulo-1 counter.

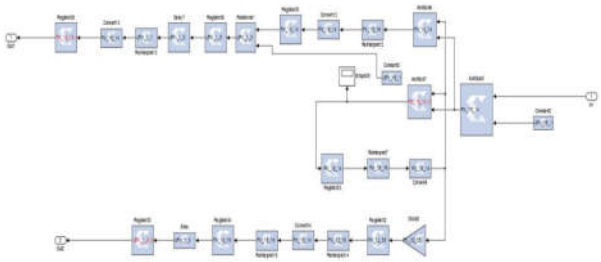

Figure 4.4. NCO in symbol timing recovery loop

5. Simulation Results

Xilinx System Generator provides a set of Simulink blocks (models) for several hardware operations that could be implemented on various Xilinx FPGAs. These blocks can be used to simulate the functionality of the hardware system using Simulink environment.

Below are the results of Modem System of Symbol Synchronizer with Garden Algorithm.

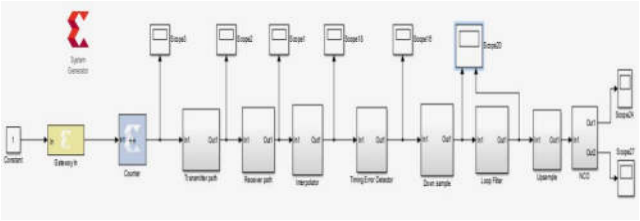

Figure 5.1. BPSK Modem System

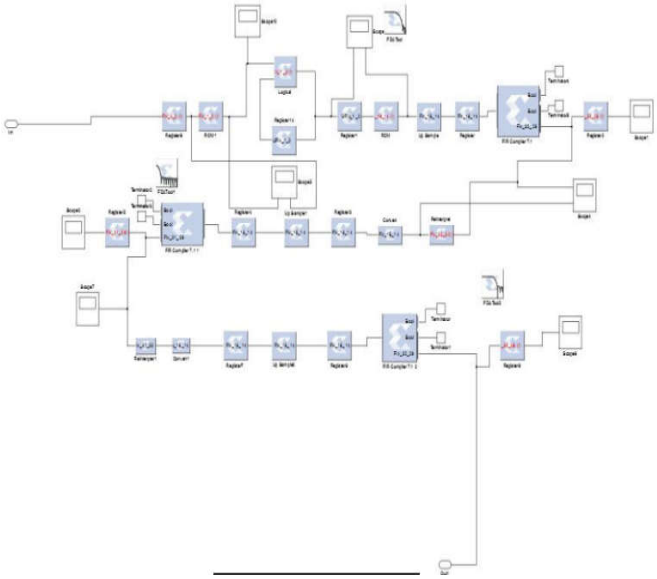

Figure 5.2. BPSK Transmitter Path

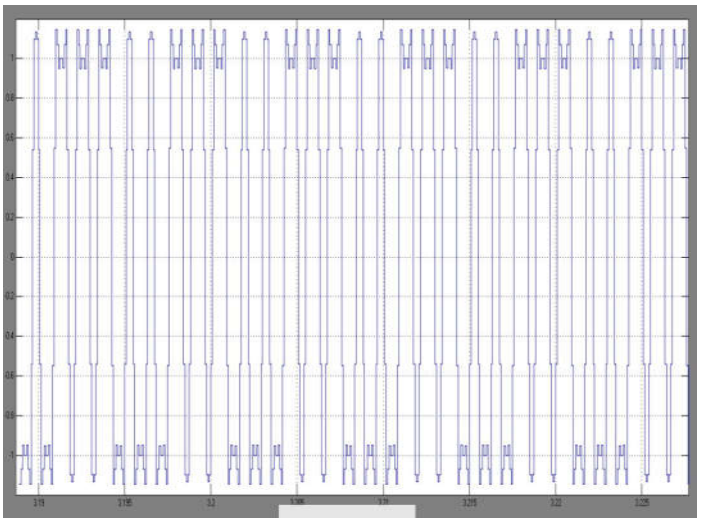

Figure 5.3. Upsampling Output for Factor of 5 in Transmission Path

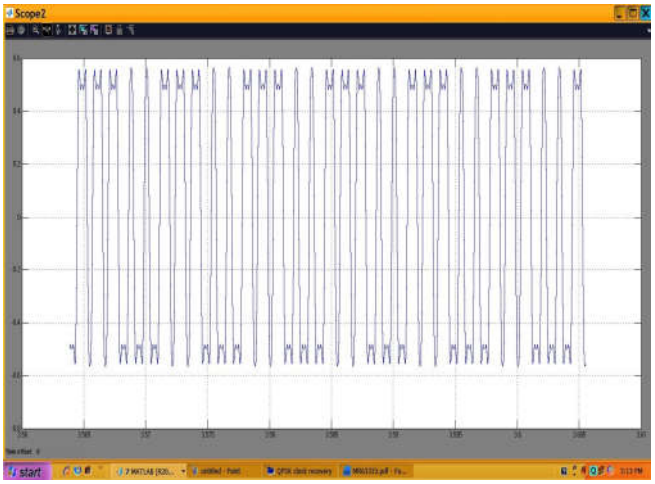

Figure 5.4. Upsampling Output for Factor of 10 in Transmission Path

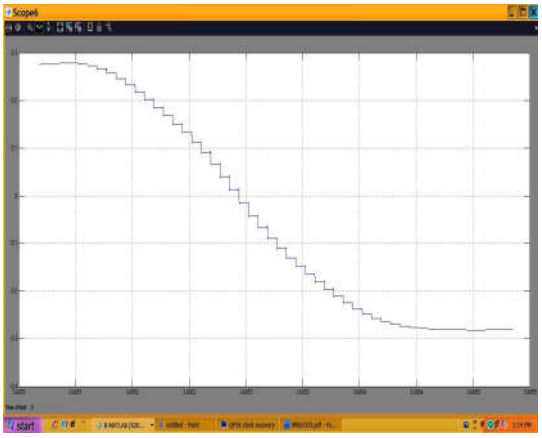

Figure 5.5. Upsampling Output for Factor of 100 in Transmission Path

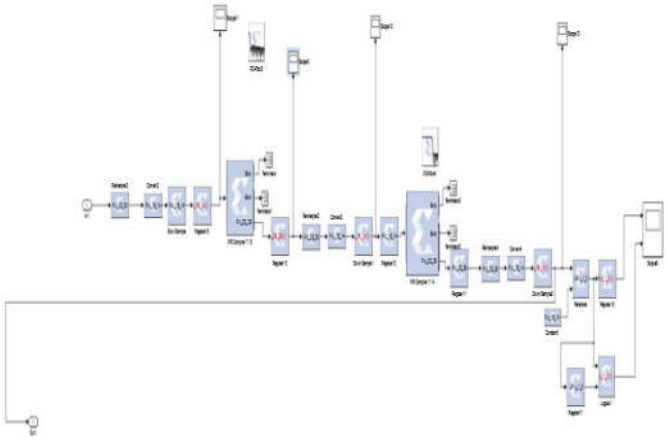

Figure 5.6. BPSK Receiver Path

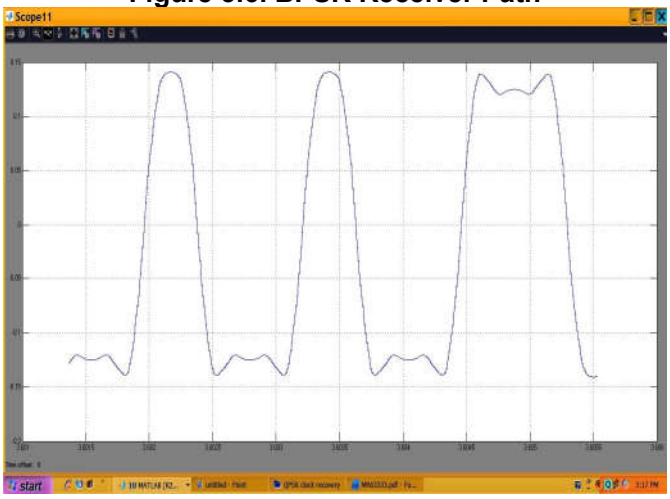

Figure 5.7. Down sampling Output for Factor of 10 in Receiver path

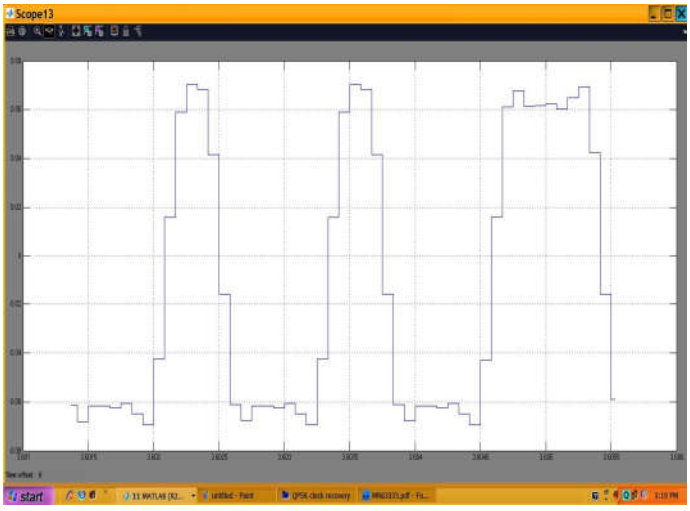

Figure 5.8. Down sampling Output for Factor of 100 in Receiver path

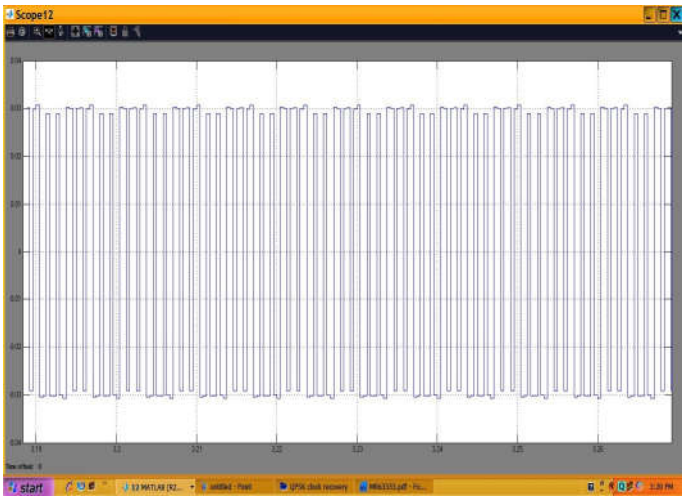

Figure 5.9. Down sampling Output for Factor of 5 in Receiver path

Figure 5.10. Receiver Output

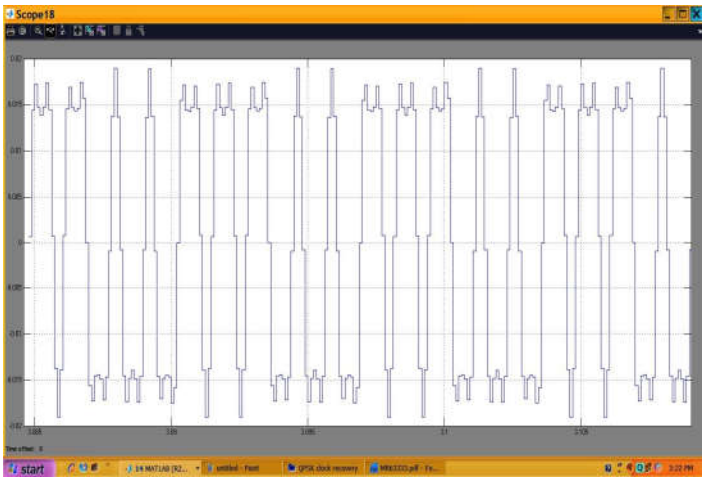

Figure 5.11. Interpolator Output

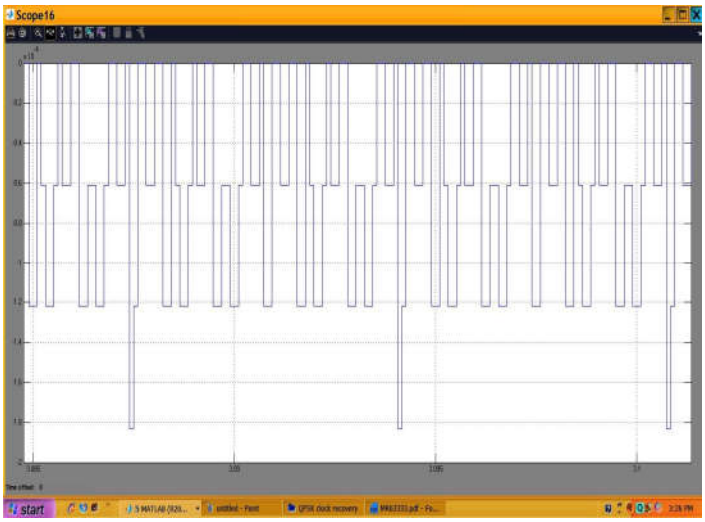

Figure 5.12. Timing Error Detector Output

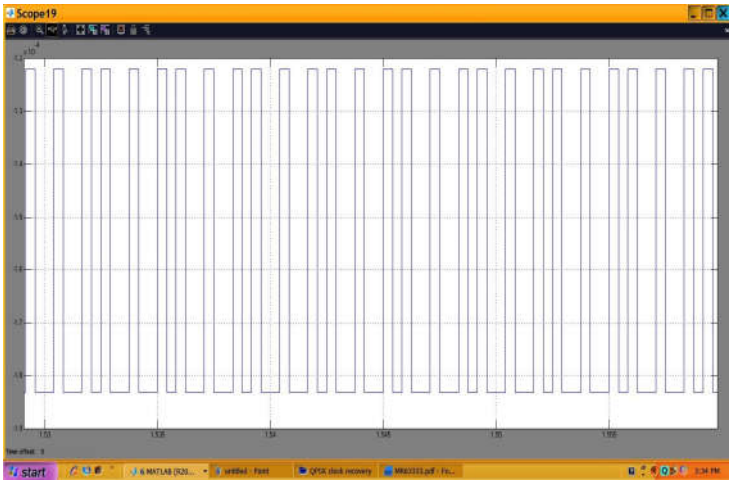

Figure 5.13. Loop Filter Output

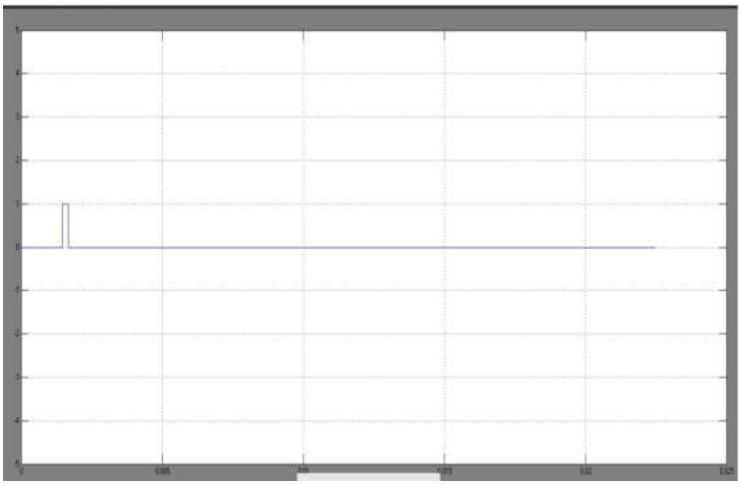

Figure 5.14. NCO output

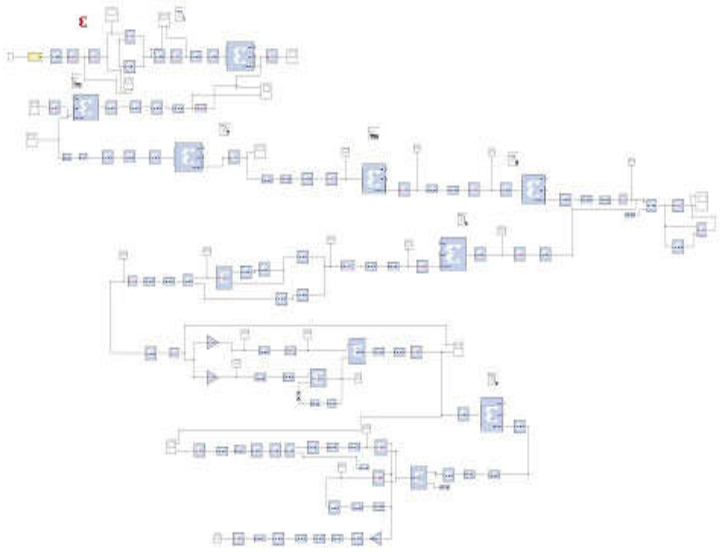

Figure 5.15. Modem System Design with System Generator Blocks

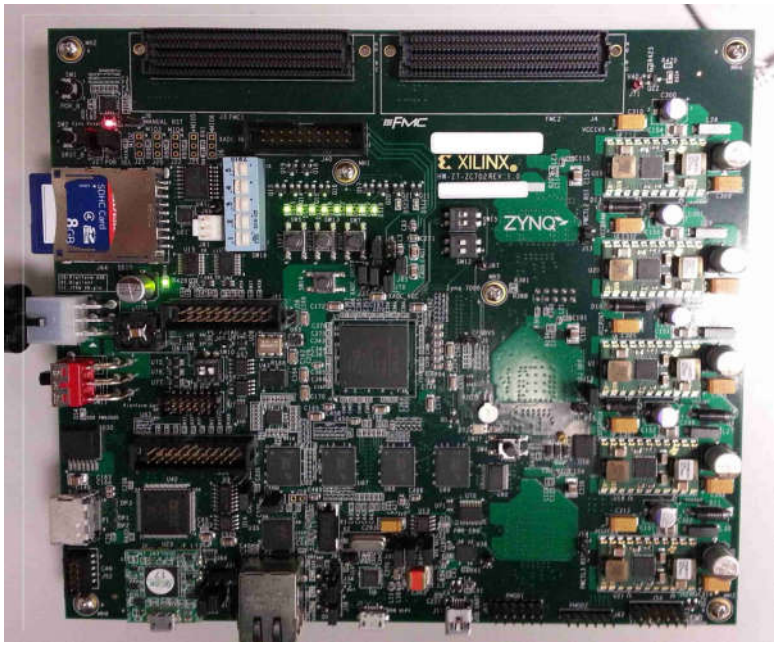

Figure 5.16. Design Implementation on ZC702 Zynq-70000 Board

6. Conclusion

This project describes an approach to implement the gardener symbol synchronizer onto a Xilinx based ZYNQ platform. It is widely used in communication systems to synchronize the transmitter and receiver clocks and it uses two samples per symbol for synchronization. The Algorithm is simulated using System Generator, where the output values have matched with the expected values based on a test input. Then the design is synthesized using Hardware Co-Simulation of System Generator. The proposed Algorithm is ported and successfully tested on Zynq development board. Implementing the Gardener symbol synchronizer within a ZYNQ SoC, lowers the number of cards in a system and is cost effective. This approach is not only very cost- effective, it also provides the added

computing power. The target system selected was a ZYNQ ZC702. Finally the resulting bit streams have been downloaded onto the ZYNQ platform in order to verify the design and the expected results were obtained.

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