FAULT TOLERANT ADAPTIVE LOGIC SRAM DESIGN USING LBIST

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ABSTRACT: In industry, chips become more and more complicated as advancing in deep submicron silicon process technology. Logic built-in-self-test (LBIST) can cover some newly emerging faults missed by traditional Automatic test pattern generation (ATPG). That's why LBIST is becoming more and more popular. Besides launching LBIST, CPU launch LBIST feature may provide more flexibility for system-level or product testing and debugging. Logic built-in self-test (LBIST) is a mechanism that lets an (IC) test the integrity of its own digital logic structures. LBIST operates by stimulating the logic-based operations of the IC and then detecting if the logic behaved as intended. The main advantage of LBIST is that it provides test capability without an external tester. In particular, safety-critical designs need to be tested and retested in a system or board. To initiate testing, an LBIST engine inside the chip requires only an access mechanism like a TAP (test access port). When a device is powered on, LBIST can also check that the logic is working properly before starting any functional tests. LBIST also decreases test cost by shortening test-cycle duration and by reducing the complexity of the test/probe setup, since the number of I/O signals that must be driven and examined under tester control is usually smaller.

KEY WORDS: LBIST, pseudo-random pattern, LFSR, MISR, in-field test

I.INTRODUCTION

Generally in battery powered applications like handled smart devices and implant medical devices the low power operations are the major problems associated with system on chip (SOC). Later this low power system on chips is realized with the low power static random access memory. In this SRAM effects the total power of SOC and occupies the large portion of area of SOC. Because of this there is reduction in power and low operating voltage effects the variations in threshold voltage. To obtain high density integration, in SRAM cell small transistors are used.

Coming to the 6T SRAM, it consists of both read and writes stability in low voltage region. The main advantage of adding decoupled read port is that it eliminates the trade-off between read stability and write stability. There are soft errors occurred in the SRAM cell, to Delimitate these errors we use the bit interleaving SRAM architecture.

The linear feedback shift register (LFSR) is most frequently used as a test pattern generator (TPG) in low area overhead built in self-test. BIST procedure can adequately reduce the adversity and intricacy of VLSI testing, by considering this actuality that an LFSR can be made with slight area overhead and decreases switching activity. In typical BIST architecture, the LFSR is frequently used in test pattern generation and output analyser. The leading fault of this architecture is that pseudorandom Patterns generated by LFSR lead to extremely high switching activities in circuit-under-test (CUT) which can motive redundant power dissipation. BIST is a design-for-testability approach that places the testing behaviour physically with the circuit under test (CUT). LFSR are the sequential logic circuits used to create pseudorandom binary sequences (PRBS) s. Built in Self-Test (BIST) is a test approach in VLSI testing. In earlier BIST architectures, the linear feedback shift register (LFSR) is generally used for test pattern generation. Major disadvantage of this methodology is the transition between the test vectors are greater and absorb high power. LFSR switching activities can purpose dynamic power dissipation.

Logic built-in-self-test (LBIST) offers a number of benefits, including the elimination of automatic test equipment's (ATEs) and at-speed testing of circuits. However, poor diagnosability is a major

drawback of LBIST. We believe that a diagnosis friendly LBIST architecture will render LBIST to be more widely adoptable. In LBIST, output compression is used to reduce the overhead of storing the fault-free responses. Multiple Input Signature Register (MISR) is one of the most popular techniques for output response compression as it converts all the fault-free responses into one final signature. Although this reduces the hardware overhead significantly, it makes diagnosis extremely difficult because if the chip fails, the diagnosis has to be performed based on a single faulty signature. Determining the root-cause based on single signature is extremely hard as the failing vector and the outputs where the fault effect propagated are unknown. Furthermore, the compressed signature is prone to aliasing and fault masking which further complicates diagnosis.

Much work has been done in the past on diagnosis of circuits containing BIST and MISR structures. In all of these techniques, multiple BIST sessions are used. In the first session, the good chips are separated from the failing chips. The defective chips are then again subject to multiple BIST sessions for diagnosis. In these sessions, diagnosis is conducted by either extracting the responses before compression or by applying new vectors to distinguish between different faults, making diagnosis a tedious and time consuming task. The speed and the power are two crucial factors for future cryptographic systems, since they are expected to support very high data rates in 5G ultra-low power products and applications.

For example, suppose that the output of a pseudo-random pattern generator used in a stream cipher is stuck to the logic 0. A stream cipher encrypts a message by combining it with a pseudo-random pattern, typically by a bit-wise addition modulo 2. In this we present a new method for LBIST which makes possible detecting stuck-at fault type of Trojans. The presented method specifically targets FSR-based cryptographic systems. In this we are going to discuss about the proposed SRAM architecture which oversees the delay in previous technology. The proposed differential architecture resolves the half select issues without the need of write back scheme. In this we use local bit line to enable the smaller delay which is obtained in circuits. At last in this paper we discuss about the SRAM technology which is used in LBIST. In this technolgy it performs both read and write operation.

II. RELATED WORK

In this bit interleaved architecture we select the SRAM cells which are used to read and write the operation. Basicakky there are two selected cells one is row half selected cell and other is column half selected cells. This target to detect/diagnose the fault in SRAM and SRAM based FPGA wherein test the logic block and all types of interconnect resources. This also covers a wide range of testing where it tests the whole architecture to diagnose fault by comparing the output of resource analyser with the standard outputs.

A hybrid framework was not sufficient for achieving fault detection, classification, and location, simultaneously.

- The impact on execution time and memory occupation of the hybrid techniques while keeping the fault detection rates same are the crucial aspects.
- For designs containing both synchronous and asynchronous clock domains, a hybrid clocking scheme using aligned double-capture and staggered double-capture was useful but not sufficient.
- Results demonstrated the possibility of employing more flexible fault tolerant techniques to SRAM based FPGAs with a high detection rate.
- The hybrid solution is more effective than the existing programmable BIST and

it is flexible enough for the test development of advanced fabrication process especially for the multi-port memories.

• In a proposed hybrid architecture the advantages of two traditional architectures, i.e. MEM-based and MUX-based LUT design architecture, for the input expansion in LUT (look up table) design but it is increasing the cost.

• As the hardware architecture for implementing the memory algorithms only March C- is used as the test for easy comparison.

• A Cyclone-II development board is also incorporated to provide a graphical user interface (GUI) on a touch LCD panel that shows the diagnosis results yielded by the presented system but it is not cost effective.

• MUX-based LUT design architecture has main advantages of hardwired connection that provide better performance but at expense of area whereas when dealing with submicron technologies MEM based architecture gave better power-area performance trade-off.

• Detecting inter-port faults in multi-port memories is a big challenge to memory testing when this kind of memories is becoming more popular in system-on chip (SOC) applications.

• The RTL code was synthesized into a gate- level netlist to estimate the hardware overhead using cell library but further modification were required.

Accumulator based and LUT based design is preferred from MUX based design. Where cost is not important SRAM based design is preferred with battery backup facility. The following points are noted to start the further work:

• The Memory BIST approach should be selected with SRAM for better fault tolerant system design.

• March C, Y Algorithms are good for Memory Testing.

• Self-healing hardware structure that can able to recover from faults generated from SEUs could be designed.

• To make the initialization more effective and accurate the un-scanned flip-flop in a tested design must be checked and initialized then the initialization of response signature register is start.

III. EXISTED SYSTEM

The task of testing a VLSI chip to guarantee its functionality is extremely complex and often very time consuming. In addition to the problem of testing the chips themselves, the incorporation of the chips into systems has caused test generation's cost to grow exponentially. A widely accepted approach to deal with the testing problem at the chip level is to incorporate built-in self-test (BIST) capability inside a chip. This increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier. In conventional testing, test patterns are generated externally by using computer-aided design (CAD) tools.

The test patterns and the expected responses of the circuit under test to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses match the expected ones. On the other hand, in BIST, the test pattern generation and the output response evaluation are done on chip thus; the use of expensive ATE machines to test chips can be avoided. This target to detect/diagnose the fault in SRAM and SRAM based FPGA wherein test the logic block and all types of interconnect resources. This also covers a wide range of testing where it tests the whole architecture to diagnose fault by comparing the output of resource analyser with the standard outputs that is available with the FPGA vendors.

The below figure (1) shows the architecture of existed system. The problem of detecting faults in SRAM-

based FPGAs is that common time redundancy methods able to detect transient faults are not applicable in this case, because an upset in the programmable matrix has a permanent effect, changing the construction of the user's combinational logic.

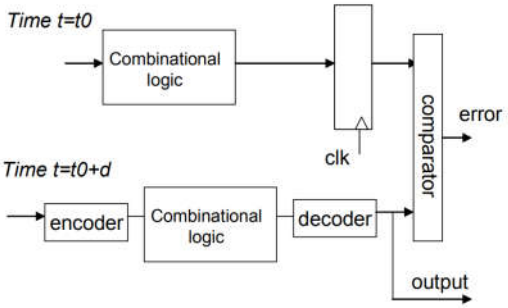


FIG.1: EXISTED SYSTEM

To allow redundancy to detect permanent faults, the repeated computations are performed differently. During the first computation at time t0, the operands are used directly in the combinational block and the result is stored for further comparison. During the second computation at time t0+d, the operands are modified, prior to use, in such a way that errors resulting from permanent faults in the combinational logic are different in the first calculation than in the second and can be detected when results are compared. These modifications are seen as encode and decode processes. But this system does not gives effectiveresults.so a new system is proposed which is discussed in below section.

IV. PROPOSED SYSTEM

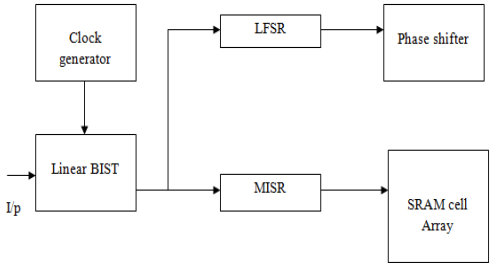


FIG.2: PROPOSED SYSTEM

The above figure (2) shows the architecture of proposed system. The components used in above block diagram are clock generator, Linear BIST, LFSR, MISR, phase shifter and SRAM cell array. PRPG gives test upgrades to filter input while MISR reduced test reaction from essential output and sweep output. Essential sources of input are controlled to esteem under Logic BIST mode. The LFSR/MISR sets are created dependent on clock space. Clock control generator is utilized to produce test clock for moving and catching Logic BIST. The FSM in focal LBIST controller will control clock control generator to create clock beat by the LBIST arrangement. The LBIST setting is configurable with the CSC (configuration shift chain) which works at TCK clock area. When the ECO occurs in the domain, the LBIST needn't do any ECO since every one of these qualities are configurable.

LBIST is not exactly the power overwhelmed by typical LFSR and yield dynamic power is diminished. Any X-source can determine the mark signature LBIST, so X-source blocking is the most basic undertaking. To enhance the test quality, the pulse number is configurable in the LBIST engineering. It's a piece of the CSC (configuration shift chain). The FSM in clock control generator can create move/catch windows for each clock area with working with focal LBIST controller. In capture window, the pulse number can be set for various test circumstance. The main advantage compared to other is that it stores multiple bits at a time in one block. Depending upon the number of bits the minimum operating voltage and area per bit vale is set. In this proposed SRAM architecture consists of single nMOS which used to buffer the read operation to increase the read current. In this buffer foot is used to reduce the leakage of SRAM cell. In SRAM cell are two selected blocks, one selected block is BLK consists of 0v and coming to another selected block that is WL remains constant. Coming to the selected block WWL is at input Vdd because of it the transistors are in on position and WBLs are set at certain voltage level. Basically

write operation consists of storage nodes and these storage nodes are connected to the WBLs.This WBLs consists of both pass gate transistors and write access transistors. At last compared to existed system, proposed system gives effective results.

V. RESULTS

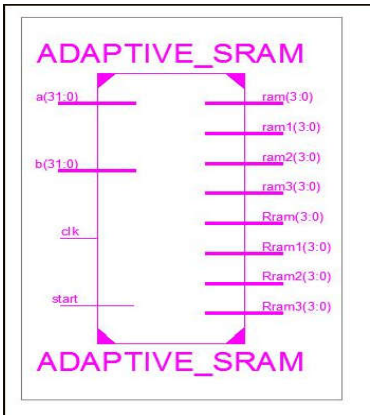


FIG.3: RTL SCHEMATIC

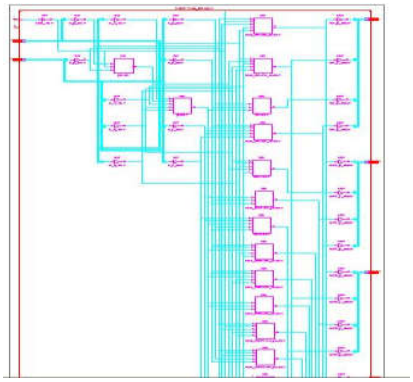
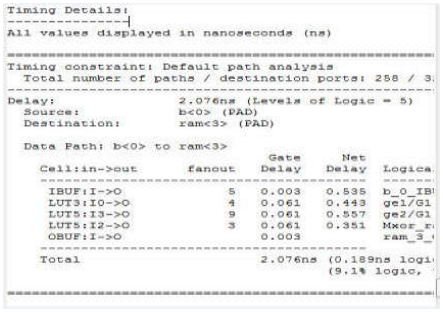


FIG.4: TECHNOLOGY SCHEMATIC

FIG.5: OUTPUT



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Timing Details:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 258 / 3
-------------------------------------------------------------------------
Delay:               2.076ns (Levels of Logic = 5)
  Source:            b<0> (PAD)
  Destination:       ram<3> (PAD)

  Data Path: b<0> to ram<3>
                              Gate     Net
    Cell:in->out      fanout  Delay    Delay  Logica
    ---------------------------------------------------
     IBUF:I->O             5    0.003   0.535  b_0_IB
     LUT3:I0->O            4    0.061   0.443  ge1/G1
     LUT5:I3->O            9    0.061   0.557  ge2/G1
     LUT5:I2->O            3    0.061   0.351  Mxor_r
     OBUF:I->O                  0.003          ram_3_
    ---------------------------------------------------
    Total                       2.076ns (0.189ns logi
                                        (9.1% logic,
=========================================================================
```

FIG.6: REPORT

VI.CONCLUSION

This algorithm is quite fast and can provide excellent solutions in short run-times. Experimental results indicate that this flow can save the designer many days of work by offering good BIST architectures which are complete in terms of logical and physical attributes. LBIST designed here using algorithm tests faster than the previously proposed ones. The main advantage of LBIST is that it provides test capability without an external tester. Compared with currently known microcode-based BIST techniques, the proposed design requires only one third of those microcode storages and the testing time is reduced. This BIST can be widely used for the embedded memory testing especially under the SoC design environment due to the superior flexibility and extendibility in applying different combination of memory test algorithms.

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