# Design And Simulation of Built-In-Self-Test (Bist) Enabled Uart

**Anusha Kadiyam[1] , Md.Shazia Fatima[2]**
[1,2]Assistant Professor ,department of ECE
Sree Dattha Institute of Engineering & Science, Hyderabad

**ABSTRACT:** In today's life the most manufacturing process are extremely complex, including manufactures to consider testability as a requirement to assure the reliability and functionality of each of their designed circuits. One of the most popular test techniques is called built-in –self-test (BIST). BIST is a design technique that allows a system to test automatically itself with slightly larger system size. a universal asynchronous receiver and transmitter(UART) with enabled BIST capability has the objective of testing the UART on chip itself and no external devices are required to perform the test. This paper focuses on the TPG (test pattern generator) circuit of BIST, in this paper, the simulation result performance achieved by BIST enabled UART architecture through VHDL programming is enough to compensate the extra hardware needed in the BIST architecture. This technique generate random test pattern automatically, so it can provide less test time compared to an externally applied test pattern and helps to achieve much more productivity at the end. In this project, the protocol of BIST Enabled UART is studied. The BIST Enabled UART architecture will be designed. Various blocks of BIST Enabled UART are modeled in VHDL. The design is functionally verified by simulating the code in ModelSim from Mentor Graphics. The FPGA synthesis is done using Xilinx ISE tool.

**Keywords:** VLSI, BIST, UART, VHDL, Cellular automata.

## I. INTRODUCTION

Testing of integrated circuits (ICs) is of vital significance to affirm an abnormal state of value in item common sense in each financially and in camera made stock. The effect of testing influences territories of creating additionally as those worried in style. This need to understand a best quality level ought to be tempered with the esteem and time worried amid this technique.

In VLSI we've testing issues like information combinatorial issues, entryway to I/O stick size connection issues, investigate age issues, light-radiating diode the architect to spot dependable investigate ways and settle this issues.teh addition of unique investigate electronic hardware on the VLSI circuits that empowers sparing investigate ways. This has been self-tended to by the prerequisite for style for testability (DFT) and subsequently the necessity for BIST. It tests the circuit or framework performs itself hence it's named as "individual test". BIST is AN on-chip investigate rationale that is used to check the valuable rationale of a chip, by it. Because of the expedient increment inside the style quality, BIST has turned into a genuine style thought in DFT ways and is changing into continuously indispensable in the present cutting edge SoCs.

An appropriately composed BIST is in a situation to balance the estimation of extra investigate equipment though at indistinguishable time making certain the trustworthiness, lessens support esteem and testability. In parallel correspondence the esteem still as nature of the framework will build as a result of simultaneous transmission of information bits on various wires. Serial correspondence mitigates this drawback and rises as viable method in a few applications for long separation correspondence since it lessens the flag bending inferable from its clear structure. All universal Asynchronous Receiver Transmitter (UART) might be a sort of serial correspondence convention.

The Universal Asynchronous Receiver Transmitter (UART) might be an in vogue and broadly utilized gadget for computerized correspondence inside the field of media transmission. Its few endowments like basic assets, solid execution, hearty hostile to sticking ability, clear to work and notice so on The UART might be a monster scale PC circuit that contains all the product framework programming important to totally control the port of a PC (Personnel PC). UART performs parallel-to-serial transformation on data character got from the host processor into serial data stream, and serial-to-parallel change on serial data bits got from serial gadget to the host processor. It moreover includes the begin and stop bit to the data for synchronization. Also to the principal occupation of changing data from parallel to serial for transmission and from serial to parallel on gathering, a UART can some of the time give additional circuits for signals that can be acclimated show the condition of the transmission media and to deal with the stream of data inside the occasion that the remote gadget isn't prepared to simply acknowledge extra data.

## 2. GENERAL BIST ARCHITECTURE

Built in-self test is a plan procedure in which parts of a circuit are utilized to test the circuit itself. Essential reason for BIST is to diminish the multifaceted nature, and in this way diminish the cost and to decrease the utilization of outer test parts. BIST comprises of LFSR, a circuit to be tried, test reaction analyzer and a BIST controller unit. BIST engineering it by and large comprises of a following segments which is appeared in Fig 1:

**Circuit under Test:** It is a part of the circuit that is to be tested in BIST mode, which can be sequential or combinational.

**Test Pattern Generator:** The Test Pattern generator is a circuit which is to be tried. It can be a chip or a committed circuit. The examples can be produced in a pseudo irregular manner or deterministically.

**Test Response Analysis:** It investigations the right estimation of arrangement on essential yield and after that contrasts it and the normal one.

**BIST Controller Unit (BCU):** BIST controller unit it controls the test execution and it handles the TPG, TRA and reconfigures the CUT and the multiplexer.

Practically UART comprises of following segments

- UART Transmitter
- UART Receiver
- Baud Rate Generator

As appeared in Fig 2 the UART transmitter module comprises of a yield enlist, a transmitter enroll and transmitter control rationale where as UART recipient module comprises of info enlist, enlist cradle enlist and beneficiary control rationale. Baud rate Generator used to create the baud rates for both the transmitter and collector.

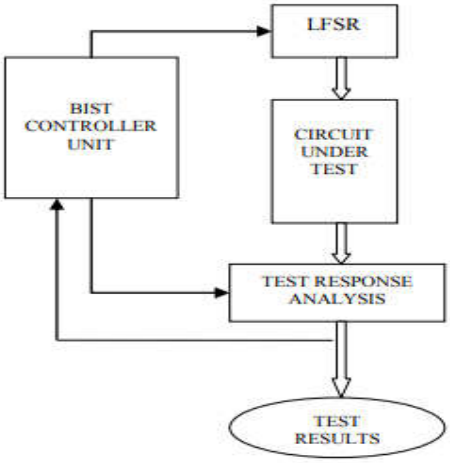



Fig 1: BIST Architecture

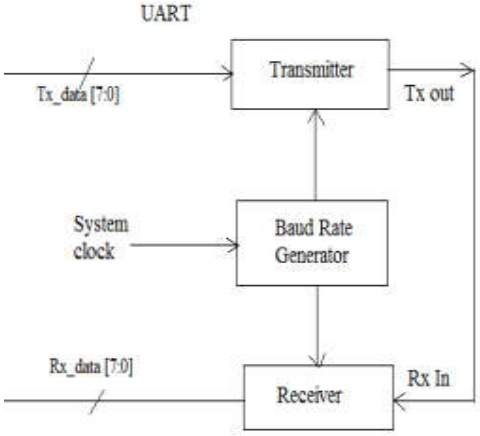



Fig 2: UART Block Diagram

## 3. PROPOSED METHOD

In this paper, we propose a novel, adaptable way to deal with diminish PD during catch periods of output based LBIST, in this manner lessening the likelihood to produce false test falls flat amid test. Like the arrangements in [8] and [11], our approach diminishes the AF of the CUT contrasted and regular sweep based LBIST, by appropriately changing the test vectors produced by the Linear Feedback Shift Register (LFSR). Our approach is by one means or another like reseeding systems (e.g., that in [22]), to the degree that the sequence of test vectors is properly modified in order to fulfill a given requirement that, however, is not to increase FC (as it is usually the case for reseeding), but to reduce PD. The basic idea behind our approach (in its nonscalable version) was introduced in [23].

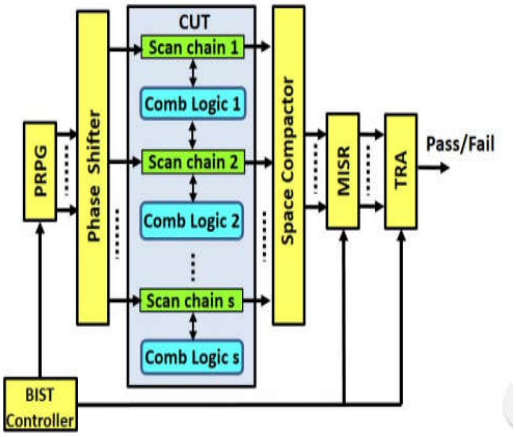



Fig. 3. Schematic of the proposed UART-based LBIST architecture.

In our proposed adaptable approach, (at least one) test vector(s) to be connected to the CUT by ordinary scanbased LBIST is (are) supplanted by new, appropriate test vector(s), hereinafter alluded to as substitute test (ST) vector(s). The ST vector(s) is (are) produced in view of the test vectors to be connected at past and future catch stages with a specific end goal to diminish the greatest number of changes between any two after test vectors. Thusly, the CUT AF and PD are diminished contrasted and the first test grouping [11]. We think about the nearness of a stage shifter (PS), which is typically received in examine based LBIST to lessen the relationship among the test vectors connected to adjoining check chains [10]. As appeared in [2], all test vectors to be connected at past and future catch stages to any sweep chain are normally given at legitimate yields of the PS, or the PS can be effortlessly changed to give them. In our approach, this property is abused to empower its ease equipment usage. Notwithstanding, our approach can likewise be embraced if the PS does not give the past and future test vectors for all output chains or if the sweep based LBIST does not present a PS.

Our approach is scalable in the achievable PD reduction. Therefore, test engineers could choose the proper AF in order to avoid the following:

1) faulty chips being tested as good (due to an induced too low AF, lower than that experienced during normal operation);

2) good chips being tested as faulty (due to an induced excessive AF, higher than that experienced during normal operation).

PD scalability is obtained by scaling the number of ST vectors to be applied between original test vectors. We will prove that our approach can reduce the maximum AF between the following capture phases from 50% (one ST vector only) to 89% (10 ST vectors) compared with conventional scanbased LBIST. This is achieved without increasing the number of test vectors (thus TT) over conventional scan-based LBIST, for a given target FC. Moreover, our approach requires a very limited area overhead (AO) compared with conventional scan-based LBIST, which ranges from approximately 1.5% (1 ST vector) to approximately 14% (10 ST vectors). In addition, our solution requires substantially less test vectors (thus TT) to achieve a target FC compared with the alternative solutions in [9] and [21].

## 4. SIMULATION RESULTS

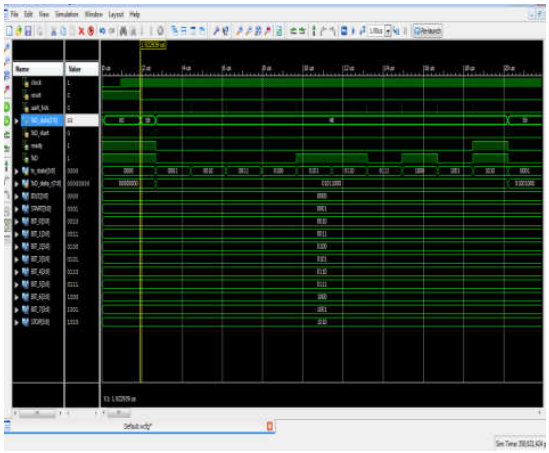


Fig 4.1: Simulated Behavioral Model of Transmitter

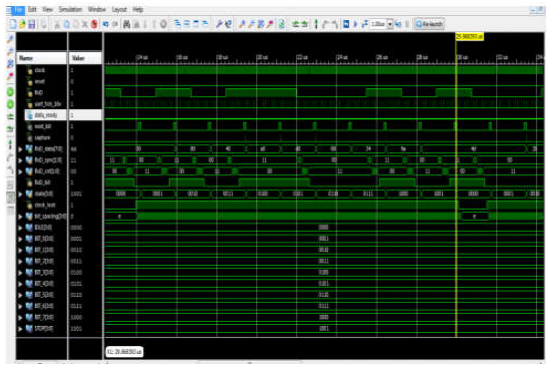


Fig 4.2: Simulated Behavioral Model of Receiver

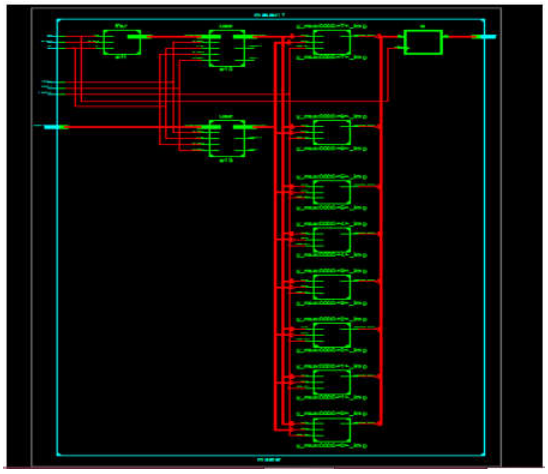
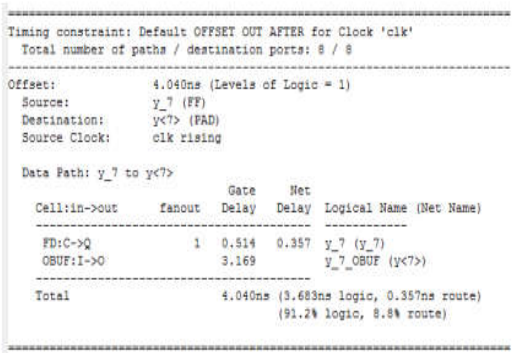


Fig 4.3: RTL Schematic.

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 67 | 4656 | 1% |
| Number of Slice Flip Flops | 86 | 9312 | 0% |
| Number of 4 input LUTs | 119 | 9312 | 1% |
| Number of bonded IOBs | 21 | 232 | 9% |
| Number of GCLKs | 2 | 24 | 8% |

Fig 4.4: Design Summary.



```
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 8 / 8
--------------------------------------------------------------------------------
Offset:              4.040ns (Levels of Logic = 1)
  Source:            y_7 (FF)
  Destination:       y<7> (PAD)
  Source Clock:      clk rising

  Data Path: y_7 to y<7>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               1   0.514   0.357  y_7 (y_7)
     OBUF:I->O                 3.169          y_7_OBUF (y<7>)
    ----------------------------------------
    Total                      4.040ns (3.683ns logic, 0.357ns route)
                                       (91.2% logic, 8.8% route)

================================================================================
```

Fig 4.5: Timing Summary.

## 5. CONCLUSION

The architecture of UART that support 8-bit data for serial transmission of data with the addition of status register for detecting errors in data transfer and BIST which allows to test the circuit itself, is introduced. Working of UART has been tested using Xilinx ISE simulator, which is implemented on FPGA. With error checking status register, we can detect the different types of errors occurred during communication and hence correct them. With the implementation of BIST, expensive tester requirements and testing procedures starting from circuit or logic level to field level testing are minimized. The LFSR replaces the function of the external tester features such as a test pattern generator by automatically generating pseudo random patterns to give good fault coverage to the UART module. Although the additional BIST circuit increases the hardware overhead and design time, it eliminates the need to acquire high-end testers. The reduction of the test cost helps in the reduction of overall production cost.

## REFERENCES

[1] Mohd Yamani Idna Idris, Mashkuri Yaacob, Zaidi Razak, “A VHDL Implementation Of UART Design with BIST capability”

[2] Dr. T.V.S.P. Gupta, Y. Kumari,M.Asok Kumar”UART realization with BIST architecture using VHDL” International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 1, January -February 2013, pp.636-640

[3] M.S. Harvey,Generic UART Manual,Silicon Valley,December 1999

[4] P. J. Anderson , “The designer’s guide to VHDL” , Morgan Kaufman , 2nd edition, 2002.

[5] Neil H.E. Weste, Kim Haase, David Harris , A. Banerjee , “CMOS VLSI Design: A circuits and Systems Perspective”, Pearson Education.

[6] K. Zarrineh, and S. J. Upadhyaya, “On programmable memory built-in self test architectures”, Design, Automation and Test in Europe Conference and Exhibition 1999. Proceedings , 1999, pp. 708 -713.