# A Novel Soft-Switched Auxiliary electrical circuit of a PFC ZVT-PWM Boost convertor for Associate in Nursing Integrated Multichip module Fabrication

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*Abstract*— this paper proposes a novel delicate exchanged helper thunderous circuit to give a zero-voltage progress at turn on for a regular pulse width-adjusted lift converter in a power factor remedy (PFC) application. The proposed auxiliary circuit empowers a fundamental switch of the lift converter to turn on under a zerovoltage exchanging condition and all the while accomplishes both delicate exchanged turn on and kill. In addition, with the end goal of a wise multichip control module manufacture, the proposed circuit is intended to fulfill a few plan limitations, including space sparing, minimal effort, and simple creation. Therefore, the circuit is effectively acknowledged by a low-appraised MOSFET and a little inductor. Nitty gritty activity and the circuit waveform are theoretically clarified, and afterward reenactment and test results are given dependent on a 1.8-kW model PFC help converter so as to check the viability of the proposed circuit.

*Index Terms*—Auxiliary resonant circuit, intelligent multi-chip power module, power factor correction (PFC), pulse widthmodulated (PWM) boost converter, zero-voltage transition (ZVT).

#### I. INTRODUCTION

POWER converters are growing very rapidly for different applications, for example, control factor revision (PFC) and exchanged mode control supply. One noteworthy power driving this improvement is the development of incredible and financially savvy coordinated power multichip modules, in light of the new ideas of building structure and propelled pressing innovation [1]– [3]. This prompts a few execution upgrades in power converters, for example, high proficiency, high power thickness, and long haul unwavering quality, with diminishing converter cost.

In addition, different converter systems and topologies have been proposed and utilized so as to enhance converter execution. One broadly utilized strategy is delicate exchanging, which creates electrical reverberation between a capacitor and an inductor amid a short turn-on/off period and thusly accomplishes zero-voltage or potentially zero-flow exchanging [4]- [10]. A few advantages of this procedure incorporate enhancing proficiency, lessening pressure, and evacuating electromagnetic impedance (EMI) clamors, yet its real downside is the prerequisite for a helper circuit to make reverberation marvels at exchanging time. The necessity of the assistant circuit increments component expenses and circuit multifaceted nature of the converter framework, yet notwithstanding for applications in industry and home machines, where cost and simple creation are the most imperative parts of the structure, there are still hindrances to utilizing delicate exchanging strategies.

Lately, the coordinated multichip control module, which itself joins the previously mentioned delicate exchanging progress procedure, has been sought after due to the superior prerequisites for vitality proficiency, music, EMI, etc, because of upgraded directions from government and vitality social orders. Furthermore, other market contenders are reliably diminishing their expenses. In any case, these execution necessities are fundamentally tested in the feeling of room requirements, warm administration, staggering expenses, and cumbersome manufacture. That is, the assistant circuit to understand the delicate exchanging system in ordinary zerovoltage progress (ZVT) hardware requires no less than three segments of vast size (i.e., inductor, MOSFET, and diode), which expends excessively space and expands costs.

This paper proposes a novel helper full circuit that can be effectively joined into a multichip control module. The proposed circuit is basic, being acknowledged with a lowevaluated MOSFET and a little inductor because of full usage of the conduction opposition RDS(on) of MOSFET while professional viding ZVT turn-on exchanging for a regular pulse width-regulated (PWM) converter. In the meantime, the MOSFET of the helper circuit works under delicate exchanging conditions amid both turn-on and kill changes. What's more, by limiting the quantity of parts and the required power rating, the circuit can without much of a stretch and cost-viably be fused into multichip control modules. The working guideline and hypothetical examination of the proposed circuit are clarified in detail. We likewise give structure contemplations and test confirmation for the objective of the proposed PWM support converter for home application with PFC.



Fig. 1. Proposed ZVT-PWM boost converter topology

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## II. PRINCIPLES OF OPERATION OF THE PROPOSED ZVT-PWM BOOST CONVERTER

#### A. Circuit Scheme and Assumption

Fig. 1 demonstrates the circuit plan of the proposed ZVT-PWM support converter. This converter contrasts from the ordinary PWM support converter of a full branch, which comprises of a resounding inductor  $L_r$ , a thunderous capacitor Cr, and an assistant switch S2 (MOSFET). For the most part, helper switch S2 has a lower control rating than that of fundamental switch S1 [insulated-door bipolar transistor (IGBT)]. Thunderous capacitor Cr is the aggregate of the parasitic capacitor of S1 and others consolidating multichip module innovation.

The accompanying presumptions are made so as to effortlessly portray the relentless state examination amid one exchanging cycle.

1) Information voltage V<sub>in</sub> is steady.

2) Yield capacitor CO is adequately substantial.

3) Principle inductor Lf is adequately expansive.

4) Principle inductor Lf is a lot bigger than assistant inductor  $L_r$ .

## B. Analysis of Operation Stages

For one exchanging cycle, the proposed circuit activities can be isolated into eight phases. Waveforms and comparable circuits for each stage are appeared in Figs. 2 and 3, separately. Stage 1 [Fig. 3(a)- t0 < t < t1]: Fundamental switch S1 and assistant turn S2 are off before t0. At the point when the helper delicately turns on at t0, the assistant inductor  $L_r$  current straightly increments from 0 to I<sub>i</sub> at t<sub>1</sub>. Amid this period, diode D is directed

The time period *t*01 of this stage is given by

$$t_{01} = \frac{I_i L_r}{V_{\text{out}}}.$$
 (1)

Stage 2 [Fig. 3(b)- t1 < t < t2]: In this stage, the circuit begins to reverberate among  $L_r$  and  $C_r$ . Assistant inductor current  $I_{Lr}$  keeps on expanding up to  $I_{S2\_peak}$ .  $C_r$  is released until the reverberation conveys its voltage to zero. This resounding time span t12 is given by

$$t_{12} = \frac{\pi}{2} \sqrt{L_r C_r}.$$
 (2)

The following equation is obtained for the peak current of the auxiliary switch *Is2\_peak*:

$$I_{S2\_peak} = I_{L_r} = I_i - I_{C_r}$$
  
=  $I_i + \frac{V_{out}}{Z} \sin(\omega(t_2 - t_1))$  (3)  
where  $Z = L_r/C_r$ , and  $\omega = 1/\sqrt{L_rC_r}$ .



Fig. 2. Waveform of the proposed ZVT-PWM boost converter

Stage 3 [Fig. 3(c)- t2 < t < t3]: When the anti-parallel diode is directing, the principle switch current streams contrarily for an extremely brief time. Principle switch voltage  $V_{CE\_S1}$  is zero at t3. Primary switch S1 is turned on under the zero-voltage exchanging condition

Stage 4 [Fig. 3(d)- t3 < t < t4]: Fundamental switch current I<sub>S1</sub> increments, though assistant switch current I<sub>S2</sub> diminishes. In this way, the aggregate of both switch flows is equivalent to Ii. In this stage, IGBT and MOSFET can be changed to the voltage source  $V_{sat_S1}$  and on-obstruction  $R_{DS(on)_{S2}}$ , individually, for investigation. This is on the grounds that the normal for the present moving through the two switches is controlled by the obstruction components of each switch. The condition for current I<sub>Lr</sub> is given by

$$V_{\text{sat}\_S1} = L_r \frac{di_{Lr}}{dt_{34}} + R_{DS(\text{on})\_S2} i_{L_r}$$
(4)

at the initial condition  $I_{Lr}(t_3) = I_i$ . The solution of (4) becomes

$$I_{L_r}(t_4) = I_i e^{-\alpha t_4} + \frac{V_{\text{sat}\_S1}}{R_{DS(\text{on})\_S2}} (1 - e^{-\alpha t_4})$$
(5)

where  $\alpha = R_{DS(on)\_S2}/L_r$ . Along these lines, (5) decides how the slant of current  $I_{Lr}$  tumbles down. The slant of current  $I_{Lr}$  diminishes by the Iie- $\alpha$ t4 term amid t3-t4. Also, the uniting estimation of current  $I_{Lr}$  can be dictated by the  $V_{sat S1}/R_{DS(on) S2}(1 - e-\alpha t4)$  term at t4.



Fig. 3. Equivalent circuits during one switching cycle. (a) *Stage 1: t0-t1*. (b) *Stage 2: t1-t2*. (c) *Stage 3: t2-t3*. (d) *Stage 4: t3-t4*. (e) *Stage 5: t4-t5*. (f) *Stage 6: t5-t6*. (g) *Stage 7: t6-t7*. (h) *Stage 8: t7-t0* 

Stage 5 [Fig. 3(e)- t4 < t < t5]: Assistant switch S2 is delicately killed. The streaming current in the assistant inductor is changed over to voltage on the parasitic capacitor of S2. Helper inductor current I<sub>Lr</sub> is zero at t5. The connection among voltage and current can be spoken to by the accompanying conditions

$$v_{C_{DS}\_S2}(t_5) = L_r \frac{di_{L_r}(t_{4-5})}{dt_{4-5}}$$
  
(6)

$$i_{L_r}(t_5) = \frac{V_{\text{sat}\_S1}}{R_{DS(\text{on})\_S2}} (1 - e^{-\alpha t_{4-5}})$$
(7)

where  $R_{DS(\text{on})}$  s<sup>2</sup> · t4-5  $>> L_r$ , and t4-5 = the period from t4 to t5. Therefore, (7) can be simplified as (8) by assuming  $e^{-\alpha t_{4-5}} = e^{-\frac{R_{DS(\text{on})}{L_r}}{L_r}} \approx 0$ 

$$v_{C_{DS}\_S2}(t_5) \approx L_r \frac{V_{sat}\_S1}{R_{DS(on)}\_S2 \cdot \Delta t}$$
(8)

$$\Delta t = \pi \sqrt{L_r C_{DS} S_2} + t_{R_G \text{off} S_2}.$$
 (9)

The voltage stretch an incentive on S2 can be found by (8). From (9),  $\Delta t$  comprises of a half-cycle full time  $\pi \sqrt{(L_r * C_{DS_{S2}})}$  what's more, a killed postpone time tRG\_off\_S2. The half-cycle thunderous time is chosen by the estimations of  $L_r$  and  $C_{DS_{S2}}$ . What's more, the kill defer time is accomplished by changing the trun-off resistance  $R_{G_{off}}$  of S2. The time among  $R_{G_{off}}$  s2 and the kill defer time is a corresponding relationship. The proposed ZVT-PWM support converter is executed with little estimations of  $L_r$  and  $C_{DS_{S2}}$ . Along these lines, the full time can be irrelevant. To accomplish adequately little  $v_{CDS_{S2}}$  inside DESIGN PROCEDURE the evaluated voltage of S2,  $R_{G_{off}S2}$  is chosen to be more noteworthy than the estimation of its particulars.

| TABLE I   |  |  |  |  |
|---|--|--|--|--|
| SPECIFICATION OF THE PREPOSED ZVT-PWM BOOST CONVERTER |  |  |  |  |

| Parameters  | Description                      | Values        |  |
|-------------|----------------------------------|---------------|--|
| Vin         | Input voltage                    | 200Vac        |  |
| Vout        | Output voltage                   | 304Vdc        |  |
| Vaut_ripple | Output voltage variation         | Vout±5%       |  |
| Izrippke    | Boost inductor current variation | Ii±5%         |  |
| fune        | Input voltage frequency          | 50Hz or 60Hz  |  |
| $f_{sv}$    | Switching frequency              | 16kHz         |  |
| Paur        | System capacity                  | 1.8kW         |  |
| η           | Boost converter efficiency       | $\eta > 0.95$ |  |

Stage 6 [Fig. 3(f)- t5 < t < t6]: This stage is indistinguishable to the ordinary PWM support converter conduct. D is killed at t5. Fundamental switch S1 behaviors and Ii streams while the helper circuit is idle.

Stage 7 [Fig. 3(g)- t6 < t < t7]: At this stage, the fundamental turn is killed, and full capacitor  $C_r$  is straightly energized to Vin voltage. Diode D is turned on normally at t7.

Stage 8 [Fig. 3(h)- t7 < t < t0]: This stage is a freewheeling condition as in the regular PWM support converter. Primary switch S2 turns on again at t0, and the task mode rehashes.

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Fig. 4. Experimental circuit scheme of a 1.8-kW 16-kHz ZVT-PWM boost converter

## **III. DESIGN PROCEDURE**

# A. Specification of the Proposed ZVT-PWM Lift Converter

The plan details of a forced air system with a PFC converter are appeared Table I. A model of the proposed ZVT-PWM support converter is appeared in Figs. 4 and 5. It has been worked to check the explanatory outcomes utilizing the parts in Table II.



Fig. 5. Picture of the proposed ZVT-PWM boost converter

## B. Determination of Lf and CO

To limit both the present swell and the voltage swell, we structure Lf and CO to be as vast as could be allowed. Be that as it may, the framework cost expands as indicated by the stringency of the determination. The upgraded CO and Lf of the proposed ZVT-PWM support converter are structured by (10) and (11) as follows [11]:

$$Lf > \frac{\left(V_{\text{in(min)}}\right)^2}{2 \cdot I_{i\_\text{ripple}} \% \cdot f_{\text{sw}} \cdot P_{\text{out}} \cdot \eta} \left(1 - \frac{\sqrt{2} \cdot V_{\text{in(min)}}}{V_{\text{out}}}\right) (10)$$

$$C_O > \frac{P_{\text{out}}}{2\pi \cdot f_{\text{line}} \cdot V_{\text{out\_ripple}} \cdot V_{\text{out}}}.$$
 (11)

| TABLE II                |       |    |     |          |         |       |
|-------------------------|-------|----|-----|----------|---------|-------|
| COMPONENTS<br>CONVERTER | VALUE | OF | THE | PROPOSED | ZVT-PWM | BOOST |

| Parameters            | Description                   | Values                         |  |
|-----------------------|-------------------------------|--------------------------------|--|
| Lf                    | Boost inductance              | 4mH                            |  |
| L <sub>r</sub>        | Auxiliary inductance          | 1.5uH                          |  |
| C1                    | Main an inch (ECU140)(400ED)  | IGBT, 20A, 600V                |  |
| 51                    | Main switch(FGH40N00SFD)      | V <sub>CE(sat)</sub> =2.3V     |  |
| c-3                   | A                             | MOSFET, 11A, 900V              |  |
| 52                    | Auxiliary switch(FQA11N90)    | R <sub>DS(an)_S2</sub> =0.96 Ω |  |
| R <sub>G_off_S2</sub> | Gate off-resistance of the S2 | 130Ω                           |  |
| Co                    | Output capacitance            | 940uF(470uF*2ea)               |  |
| C <sub>r</sub>        | Auxiliary capacitance         | 2.2nF                          |  |
| BD                    | Bridge diode(GBPC3506)        | 35A, 600V                      |  |
| D                     | Main diode(RHR3060)           | 30A, 600V                      |  |

# C. Determination of S2

At the turn-on condition, assistant switch current IS2 moves through the deplete to the hotspot for a brief timeframe (a couple of microseconds) and its obligation proportion is under 0.1. In this paper, the on-time of S2 is inside 3  $\mu$ s. This plan estimation of the auxiliary switch S2 can be connected so as to choose the MOSFET (FQA11N90) gadget by utilizing the beat deplete current specifications. Ordinarily, the greatest heartbeat deplete current is around multiple times the estimation of the constant deplete current [12]. Furthermore, the anticipated estimation of IS2\_peak from (3) can be connected to choose the assistant switch. The assistant switch MOSFET ought to be more than double the determined estimation of IS2 peak while the beat deplete current is 45.6 A. So as to

accomplish a fast de-wrinkle in the slant of  $I_{S2, S2}$  is chosen to fulfill the accompanying condition:

$$V_{\text{sat}_{S1}} < I_{S_{S2}}R_{DS(\text{on})_{S2}}$$
 (12)

where *Is\_s2* is the maximum continuous drain–source forward current of *S2*. When the *RDS*(on) of *S2* is selected sufficiently large, the voltage stress of *S2* is much smaller than its rated voltage from (7).







Fig. 7. Waveforms of the 1.8-kW 16-kHz experimental proposed ZVT-PWM boost converter at full load.

#### D. Determination of Lr and Cr

To accomplish ZVT turn-on of the fundamental switch, the turn-on flag of S1 ought to be connected while its antiparallel diode is leading. Additionally,  $I_{S2\_peak}$  must be more prominent than the estimation of Ii. This esteem is dictated by  $L_r$  and  $C_r$ . From (3),  $L_r$  and  $C_r$  can be approximated.



Fig 8. Measured currents and voltages of two switches at 1.8 kW and 16 kHz.



Fig. 9. Measured current and voltage of S2 at 600 W and 16 kHz

TABLE III COMPARISON OF THE AUXILIARY CIRCUITS OF THE PROPOSED AND CONVENTIONAL TOPOLIGIES

| Parameters     | Description           | Proposed<br>Topology | Conventional<br>Topology |
|----------------|-----------------------|----------------------|--------------------------|
| Pont           | System capacity       | 1.8kW                | 600W                     |
| fsw            | Switching frequency   | 16kHz                | 100kHz                   |
| L <sub>r</sub> | Auxiliary inductance  | 1.5uH                | 16uH                     |
| C <sub>r</sub> | Auxiliary capacitance | 2.2nF                | 4.4nF                    |
| D2             | Clamped diode         | none                 | Used                     |

## IV. SIMULATIONS AND EXPERIENTAL RESULTS

## A. Simulation Results

The proposed framework is mimicked in PSIM programming. A genuine model of each power gadget is



Fig. 10. Measured currents and voltages of S1 and S2 during one switching cycle in the proposed topology at 600 W and 16 kHz. (a) Waveforms of S1. (b) Waveforms of S2.



Fig. 11. Measured currents and voltages of S1 and S2 during one switching cycle in the conventional topology at 600 W and 16 kHz. (a) Waveforms of S1. (b) Waveforms of S2.

utilized in the schematic dependent on the gadget information sheets. The mimicked waveforms of the proposed ZVT-PWM converter are appeared in Fig. 6. As can be found in the recreation results, the fundamental switch is ZVT turned on and delicately killed. The helper switch is delicately turned on and off. At the point when IS2 adequately diminishes, the voltage weight on S2 is a lot littler than the appraised voltage of S2 dependent on (7) and (8).

# B. Experimental Results

A control circuit with the DSP chip (TMS320F28335) has been utilized for this trial. The current and the voltage of the converter are detected utilizing LEM HX 20-P and LEM LV 25-P, separately.

The waveforms of the info and yield flows and voltages are appeared in Fig 7. These waveforms are estimated at the amended hub. The information current is in stage with the information voltage (PFC). In light of utilizing resistive load, yield voltage V<sub>out</sub> is acclimated to 304 V to fulfill the 1.8-kW framework limit. V<sub>out</sub> is  $304 \pm 14$  V<sub>dc</sub>, obviously. The current and voltage waveforms of primary switch S1 and helper switch S2 are appeared in Fig. 8. The principle switch is ZVT turned on, and the helper switch is delicately turned on and off. These outcomes are fundamentally the same as the recreation waveforms. Likewise, the voltage worry of S2 was estimated at 40 V<sub>peak</sub> at killed time. This esteem is a lot littler than the evaluated voltage of the helper switch. There is no extra voltage weight on S2. In Fig. 9, the voltage and current waveforms of S2 are appeared. S2 is worked an exceptionally brief time inside the obligation factor 0.05.



Fig. 12. Measurement graph of CE for the proposed topology.



Fig. 13. Measurement graph of CE for the conventional topology

# C. Comparison of the Proposed ZVT-PWM Lift Converter and the Traditional ZVT-PWM Lift Converter

Table III thinks about the helper circuits of the proposed and regular topologies. Despite a bigger limit and lower exchanging recurrence, the proposed topology utilizes littler  $L_r$  and  $C_r$  than those of the ordinary topology. Likewise, no clipped diode is utilized in the proposed topology. These favorable circumstances empower a helper circuit that is basic, little, and ease. The helper circuit very just comprises of  $L_r$ ,  $C_r$ , and S2.

Figs. 10 and 11 demonstrate the exchanging waveforms (i.e., S1 and S2) of the proposed and customary topologies. In the two cases, a similar circuit parameters, including similar estimations of  $L_r$  and  $C_r$ , are utilized, yet the framework limit is littler than 600 W contrasted and the regular one. As appeared in Fig. 10, the proposed topology gives a smooth killed waveform at S1 and S2, without voltage spikes and mutt lease ringing. Nonetheless, the regular topology, as appeared in Fig. 11, encounters a substantial voltage spike at S2 and current ringing at S1 when the S2 turn is killed. This conduct makes the proposed topology an enhanced EMI execution while giving a high converter effectiveness estimation of 97.5%.

Figs. 12 and 13 demonstrate the deliberate charts of directed outflow (CE) for the two topologies by utilizing a Rohde and Schwarz ESCI EMI test collector. When looking at the two charts, a low recurrence extend demonstrates comparative execution, yet in the high recurrence from 4 to 26 MHz, the CE of the proposed topology enhanced to 4 dB littler than the traditional topology because of the smooth exchanging transient at S1 and S2. This empowers the EMI channel configuration to fulfill the global directions of CE.

#### V. CONCLUSION

This paper has introduced another ZVT-PWM support converter with a functioning snubber. This straightforward snubber circuit can be coordinated into the multichip control module. The activity of the proposed circuit was hypothetically portrayed. As appeared, the proposed strategy has a diminished circuit unpredictability, a limited helper inductor, and decreased CE. Also, the primary and assistant changes are affirmed to have ZVT turned on and delicately turned on and off. The voltage worry of the assistant change is observed to be about 5.6%, which is very low for the proposed converter framework.

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